Texas Instruments
Tools for system-level challenges
A live demo of the top tools to help you navigate your design journey
Jason Clark // Aerospace & Defense Systems
Agenda

• TI industrial systems team overview
• Live demo to find products and reference designs for your application
• Overview of select high speed reference designs
Aerospace & Defense Systems Team Overview

• Organizational Goals
  – Solve our customer’s system-level challenges
  – Work across TI’s product lines and businesses to develop system solutions maximizing signal chain, interface and power performance
  – Demonstrate individual product(s) performance within the system environment → Beyond the EVM (e.g. how does TI’s Pwr, ISO, Protection, etc. impact performance)
  – Bring an End Equipment perspective to product roadmap definition

• Aerospace & Defense Team
  – Initiated in 2015, now at 5 System Engineers, 1 AFEs and (average YoE >15yrs)
  – Twenty six reference designs released, 9 in development!
What’s included in a reference design?

- **Design Files:**
  - Complete **design guide** outlining design features, specifications, block diagram, system design theory, hardware/software, and measured results
  - **Schematics** and **Altium or CAD files**
  - **Bill of Materials**
  - **Gerber Files**
  - **Assembly Drawings**
Where to find reference designs?

Main Library

- Located at: www.ti.com/tidesigns
- Search by keyword, application, or products

Find through Application Folders

- Located at: www.ti.com/applications
- Search by market, sector or application

Find through Product Folders

- Located at individual product pages
- Find TI Designs under the Tools & Software tab
Reference Designs for High Speed Systems
Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers - TIDA-01021

**Features**

- 15 GHz Multi-channel JESD204B complaint clocking solution,
  - Device clock frequency – LMX2594 (max – 15 GHz)
  - SYSREF provided for JESD204B interface – LMX2594
- Scalable clocking solution, which can generate various DEVCLK by LMX2594 / LMK04828
- FMC connector adaptor boards to interface with TI high speed analog front end EVMs
- Low power and highly integrated multi-channel clocking solution with JESD204B complaint

**Target Applications**

- Oscilloscope
- Wireless Communication Tester
- Software Defined Radio
- Phased Array Radar

**Tools & Resources**

- Synchronization of JESD204B Giga-Sample ADCs using Xilinx Platform for Phased Array Radar Systems
- LMX2594 – Expected RTM (Q1’17)

**Benefits**

- JESD204B compatible clocking solution for high dynamic range and high SNR multi-channel AFE signal chain
- Configurable phase synchronization to achieve low skew
- 15 GHz clocking solution can be used in multiple end equipments (DSO, Radar, Wireless Test, etc.)
- Supports low latency signal measurement and signal generation systems
Subsystem block diagram
Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers
Subsystem test setup block diagram
Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers

* Test setup block diagram for channel-to-channel skew measurement

* Test setup block diagram for SNR measurement
# Reference design results

Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers

## Table 3. Measured Phase Noise

<table>
<thead>
<tr>
<th>OUTPUT FREQUENCY (GHz)</th>
<th>CONDITION</th>
<th>EXPECTED PHASE NOISE (dBc/Hz)</th>
<th>MEASURED PHASE NOISE (dBc/Hz)</th>
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</thead>
<tbody>
<tr>
<td>3.5</td>
<td>10-kHz offset</td>
<td>-117.0</td>
<td>-118.0</td>
</tr>
<tr>
<td>100-kHz offset</td>
<td>-119.7</td>
<td>-119.3</td>
<td></td>
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<tr>
<td>1-MHz offset</td>
<td>-130.5</td>
<td>-128.7</td>
<td></td>
</tr>
<tr>
<td>10-MHz offset</td>
<td>-149.5</td>
<td>-151.5</td>
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<tr>
<td>10-kHz offset</td>
<td>-106.8</td>
<td>-108.1</td>
<td></td>
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<tr>
<td>100-kHz offset</td>
<td>-111.4</td>
<td>-110.1</td>
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<td>1-MHz offset</td>
<td>-123.1</td>
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<tr>
<td>10-MHz offset</td>
<td>-147.4</td>
<td>-147.5</td>
<td></td>
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<tr>
<td>10-kHz offset</td>
<td>-104.7</td>
<td>-103.8</td>
<td></td>
</tr>
<tr>
<td>100-kHz offset</td>
<td>-107.5</td>
<td>-105.9</td>
<td></td>
</tr>
<tr>
<td>1-MHz offset</td>
<td>-114.7</td>
<td>-115.1</td>
<td></td>
</tr>
<tr>
<td>10-MHz offset</td>
<td>-141.7</td>
<td>-140.8</td>
<td></td>
</tr>
</tbody>
</table>

## Input Freq (MHz) | ADC Datasheet SNR (dBFS) | Measured SNR on ADC12DJ3200 EVM with on board clock (dBFS) | Measured SNR on ADC12DJ3200 EVM with TIDA-01021 clocks (dBFS) |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>997</td>
<td>56.3</td>
<td>55.25</td>
<td>55.72</td>
</tr>
<tr>
<td>2482</td>
<td>55.2</td>
<td>52.71</td>
<td>53.94</td>
</tr>
<tr>
<td>5250*</td>
<td>52.6</td>
<td>50.34</td>
<td>49.6*</td>
</tr>
</tbody>
</table>

## Input Frequency (MHz) | Measured Time Skew (ps) | Average | AvgFactor | Calculator | Result |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
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<tr>
<td>997</td>
<td>9.23</td>
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<td></td>
<td></td>
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<tr>
<td>2482</td>
<td>9.35</td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers - TIDA-01023

**Features**

- Scalable 15 GHz Multi-channel JESD204B complaint clocking solution,
- Device clock frequency – LMX2594 (max – 15 GHz)
- SYSREF provided for JESD204B interface – LMX2594
- Scalable clocking solution, which can generate various DEVCLK by LMX2594 / LMK04828
- FMC connector adaptor boards to interface with TI high speed analog front end EVMs
- Low power and highly integrated multi-channel clocking solution with JESD204B complaint

**Consulting Applications**

- Oscilloscope
- Wireless Communication Tester
- Software Defined Radio
- Phased Array Radar

**Tools & Resources**

- TIDA-01021
- TSW14J56/57
- LMK04828EVM
- ADC12DJ3200EVM

**Benefits**

- JESD204B compatible clocking solution for high dynamic range and high SNR multi-channel AFE signal chain
- Configurable phase synchronization to achieve low skew
- Scalable 15 GHz clocking solution can be used in multiple end equipments (DSO, Radar, Wireless Test, etc.)
- Supports low latency signal measurement and signal generation systems
Subsystem block diagram
High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers

- Designed multi channel clocking board 1 & 2 provides the synchronized JESD204B complained clocks using the Master LMK04828, which provides the reference signals and sync signals to both clocking boards.

- Designed FMC+ adaptor boards provides the interface between TI existing HS ADC EVMs and capture cards

- Multi channel clocking board further scalable up to 7 boards, with the remaining ports of master LMK04828

- Scaling can be more by using the tree topology

- No propagation delay shift over temperature
Clock demonstration with ADC12DJ3200
High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers

- ADC12DJ3200 EVM on-board clocks are replaced with TIDA-01023 clocks
- TIDA-01023 on-board LMX2594 generates DEV_CLK – 3GHz and SYSREF – 37.5MHz
- FPGA Clocks are distributed by TIDA-01023 on-board LMK04828 (Slave)
- LMX2594 PLL Synthesizer settings are:
  - REFin – 37.5MHz
  - PD freq – 37.5MHz
- Measured system SNR is improved by the 0.2 to 0.5 dB to the ADC12DJ3200EVM performance and close to the datasheet specs

<table>
<thead>
<tr>
<th>Input Freq (MHz)</th>
<th>ADCDatasheet SNR (dBFS)</th>
<th>Measured SNR on ADC12DJ3200EVM with onboard clocks (dBFS)</th>
<th>Measured SNR on ADC12DJ3200EVM with TIDA-01023 clocks (dBFS)</th>
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<td>2482</td>
<td>55.2</td>
<td>52.71</td>
<td>53.5</td>
</tr>
</tbody>
</table>
Clock synchronization demonstration with two ADC12DJ3200 channels
High Channel Count JESD204B Clock Generation Reference Design for DSO, Radar and 5G Wireless Testers

Test setup block diagram

Measured Channel to channel skew

Sampled Signals at 997-MHz Input

Sampled Signals at 2482-MHz Input
Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems - TIDA-01024

Features

• Scalable 15 GHz Multi-channel JESD204B complaint clocking solution,
• Device clock frequency – LMX2594 (max – 15 GHz)
• SYSREF provided for JESD204B interface – LMX2594
• Scalable clocking solution, which can generate various DEVCLK by LMX2594 / LMK04828
• FMC connector adaptor boards to interface with TI high speed analog front end EVMs
• Low power and highly integrated multi-channel clocking solution with JESD204B complaint

Benefits

• JESD204B compatible clocking solution for high dynamic range and high SNR multi-channel AFE signal chain
• Configurable phase synchronization to achieve low skew
• Scalable 15 GHz clocking solution can be used in multiple end equipments (DSO, Radar, Wireless Test, etc.)
• Supports low latency signal measurement and signal generation systems

Target Applications

Oscilloscope
Wireless Communication Tester
Software Defined Radio
Phased Array Radar

Tools & Resources

• TIDA-01021
• TSW14J56/57
• LMK04828EVM
• ADC12DJ3200EVM
Subsystem block diagram
Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems

- Designed multi channel clocking board 1 & 2 provides the synchronized JESD204B complained clocks in daisy chain configuration, which get the reference signal and sync signals from the previous board.
- Designed FMC+ adaptor boards provides the interface between TI existing HS ADC EVMs and capture cards
- Multi channel clocking board further scalable without affecting the previous section of the chain
- Scaling up is more easy but it could not be use where temp drift is more which affects the reference signal feeding to each board
Clock demonstration with ADC12DJ3200
Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems

• ADC12DJ3200 EVM on-board clocks are replaced with TIDA-01024 clocks
• TIDA-01024 on-board LMX2594 generates DEV_CLK – 3GHz and SYSREF – 37.5MHz
• FPGA Clocks are distributed by TIDA-01024 on-board LMK04828 (Slave)
• LMX2594 PLL Synthesizer settings are:
  • REF in – 37.5MHz
  • PD freq – 37.5MHz
• Measured system SNR is improved by the 0.2 to 0.5 dB to the ADC12DJ3200EVM performance and close to the datasheet specs

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<thead>
<tr>
<th>Input Freq (MHz)</th>
<th>ADC Datasheet SNR (dBFS)</th>
<th>Measured SNR on ADC12DJ3200EVM with onboard clocks (dBFS)</th>
<th>Measured SNR on ADC12DJ3200EVM with TIDA-01024 clocks (dBFS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>997</td>
<td>56.3</td>
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<td>55.4</td>
</tr>
<tr>
<td>2482</td>
<td>55.2</td>
<td>52.71</td>
<td>53.38</td>
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</table>
Clock synchronization demonstration with two ADC12DJ3200 channels
Large scale multi-channel daisy chained JESD204B clocking reference design for RADAR, MIMO and 5G systems

Test Setup Block Diagram

Measured Channel to channel skew

Sampled Signals at 997-MHz Input

Sampled Signals at 2482-MHz Input
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems - **TIDA-01022**

### Features
- Flexible analog input bandwidth and sample rate for multichannel configuration
- Maximum Analog Input Bandwidth – DC to 1.5 GHz
- Analog Front End Sampling Performance
  - 3.2 Gsps (Multi-channel 4 channel)
- Pin compatible ADCs
  - ADC12DJ3200 / ADC12DJ2700 / ADC12DJ1600
- Multi-channel JESD204B complaint clocking solution to generate DEV CLK / SYSREF
  - LMK04828 with LMX2594
  - JESD204B Support
    - Connects to Next Generation High Speed ADC capture cards (TSW14J56 / TSW14J57)
    - 8/16/32 lanes options @ 12.5 Gbps

### Benefits
- High performance 12 bit analog capture
- Scalable Platform
  - Analog Input Channels (up to 4)
  - Analog input bandwidth (DC to 1.5GHz)
  - Front End Sampling clock (Up to 3.2 Gsps)
  - JESD lane support (up to 32 lanes on board)
- Integrated high speed clocking solution for multichannel synchronization.
- Support HSDC Pro GUI for Advanced system parameter Analysis

### Target Applications
- High Performance Oscilloscopes
- Wireless Communication Test Equipment
- Software Defined Radio
- RADAR

### Tools & Resources
- **TSW14J56EVM**
- **ADC12DJ3200 EVM**
  - Key parts
    - ADC12DJ3200, LMK04828, LMX2594, LMH5401, LMH6401

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![Diagram of the Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems - TIDA-01022](image-url)
System block diagram/test setup with TSW14J56
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

<table>
<thead>
<tr>
<th>Clock Solution/Interleave</th>
<th>Sampling Speed (Gsp)</th>
<th>ADC</th>
<th>No of Lane/Per Device</th>
<th>Lane Rate (Msp)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-ch On chip</td>
<td>1.6</td>
<td>2x ADC12DJ1600</td>
<td>8L</td>
<td>6400</td>
</tr>
<tr>
<td></td>
<td>2.7</td>
<td>2x ADC12DJ2700</td>
<td>8L</td>
<td>10800</td>
</tr>
<tr>
<td></td>
<td>3.0</td>
<td>2x ADC12DJ3200</td>
<td>8L</td>
<td>12800</td>
</tr>
<tr>
<td>2-ch On chip</td>
<td>3.2</td>
<td>2x ADC12DJ1600</td>
<td>8L</td>
<td>6400</td>
</tr>
<tr>
<td></td>
<td>5.4</td>
<td>2x ADC12DJ2700</td>
<td>8L</td>
<td>10800</td>
</tr>
<tr>
<td></td>
<td>6.1</td>
<td>2x ADC12DJ3200</td>
<td>8L</td>
<td>12800</td>
</tr>
<tr>
<td>1-ch On board</td>
<td>6.4</td>
<td>2x ADC12DJ1600</td>
<td>8L</td>
<td>6400</td>
</tr>
<tr>
<td></td>
<td>10.8</td>
<td>2x ADC12DJ2700</td>
<td>8L</td>
<td>10800</td>
</tr>
<tr>
<td></td>
<td>12.8 (12.3 †)</td>
<td>2x ADC12DJ3200</td>
<td>8L</td>
<td>12800</td>
</tr>
</tbody>
</table>

† Clock solution: LMK04832 alone
‡ Amplifier bypassed

Sample clock option
- 3.2 Gsp (LMK04828 + LMX2594)
Hardware setup
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

- Channels 1 & 2
- Channels 3 & 4

Clock
- LMK04828
- LMX2594
- LMK00304
- LMX2594

Amplifier
- LMH5401
- LMH6401

Data Converter
- ADC12DJ3200
- ADC12DJ3200

Capture Card
- TSW14J56/57
- TSW14J56/57

Power
- TPS7A3301 (LDO)
- TPS7A8300 (LDO)
- TPS7A8400 (LDO)
- TPS259261
- TPS82130 (DC-DC)
• Support AC and DC input coupling
• Support both single ended and differential Input
• Input Analog Bandwidth DC - 1.5GHz
• Programmable Gain up to 30.4dB (LMH5401+LMH6401)
**Clocking options – clock tree**

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

**Connector Options**

1. OSCin of LMK04828 accepts reference clock input from any one of following:
   - LMK61E2 oscillator
   - On board VCXO
   - External clock via OSCin P3 SMA connector

2. CLKIN0 accepts standard 10 MHz or 100 MHz reference from SMA connector (J26,J27)

3. CLKIN1 accepts clocks from SMA connector (J28) through clock divider, this divide by 4 clock divider useful to divide very high input clock source

4. SMA connector OSCinP1, OSCinP2 used to provide external SYSREF to LMX2594

5. SMA connector J10, J21 used to provide the DCLK to ADC1 & ADC2 directly from external clock source
• Provided optimized power solution that minimize SNR and SFDR degradation while using switching regulator.
• Optimized solution for overall system power and PCB board area.

Power supply block diagram
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

Key parts
TPS82130
TPS7A8400
TPS7A8300, TPS7A3301

TI Design planned for Q1-2018
Test results – (LMH5401 + LMH6401) input
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

Test Condition:
- ADC dual channel mode (JMODE2)
- Single channel measurement
- Sample rate 3GHz
- AIN = -1dBFS
- CH3,4 LMX2594 clock portion off
- Capture card used
  - TSW14J57

- Cascaded Amplifier Input (FDA + DVGA)
- front end provides wide dynamic range (-6 to 24.4 dB)
- Programmable gain in 1dB step
- Programmable common mode voltage

SNR, Gain vs Frequency

SFDR, Gain vs Frequency

THD, Gain vs Frequency
Test results – transformer input

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

Test Condition
- ADC Dual channel mode (JMODE2)
- Sample rate 3GHz
- AIN = -1dBFS
Test results – channel to channel skew
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

Test Condition
• Input Signal Frequency: 997 MHz
• Sampling Frequency: 2700 MHz

Test Mode
• Master slave with TSW14J56

Less than 5 psec skew

ADC2 lags ADC1 by 0.111 deg or 0.23 ps
Power solution update for ADC12DJ3200
System block diagram on board power

Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

- TPS82130 power module use
- No External Frequency SYNC
- Thermal performance is not good due to very tiny package
System block diagram with TIDA-01027
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

- TPSM84424 power module used
- External Frequency SYNC with phase shifted clock
- Thermal performance is good
- Hot rod package helps to improve EMI performance
Test results – with TIDA-01027
Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems

<table>
<thead>
<tr>
<th>Supply Rail (V)</th>
<th>Calculated Current (A)</th>
<th>Power (W)</th>
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<tbody>
<tr>
<td>1.9</td>
<td>1.9</td>
<td>3.61</td>
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<td>1.1</td>
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<td>-2.5</td>
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<td>1.40</td>
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<tr>
<td>Total Output Power</td>
<td>15.56</td>
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</table>

<table>
<thead>
<tr>
<th>Supply Rail (V)</th>
<th>Current (I)</th>
<th>Power (W)</th>
</tr>
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<tbody>
<tr>
<td>1.9</td>
<td>2.17</td>
<td>4.12</td>
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<td>2.89</td>
<td>3.18</td>
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<td>0.519</td>
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<td>-2.5</td>
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<td>1.27</td>
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<tr>
<td>Total Output Power</td>
<td>16.27</td>
<td></td>
</tr>
</tbody>
</table>

Input Supply: 12V @ 1.65A
Input Power: 19.8 W
Efficiency: 82.15%

Test Condition
• TIDA-01027 operation mode
  • LDO bypassed, DCDC + Filter Only at output
  • DCDC running free mode (No frequency SYNC across convertors)
• TIDA-01022 operation mode
  • JMODE0, Fs = 12.8 Gsps, Fin = 997MHz

Note: We are getting ≈70% efficiency in TIDA-01022 with on board power supply
Upcoming from Texas Instruments:

Power Solutions for Industrial Applications Webinar (February)
Learn about the newest ICs released from TI and how they can help you meet some of the design requirements you are facing with current and future projects.

APEC Tradeshow (March)
Meet us at APEC! Learn how TI is helping engineers achieve leadership in power density and solve tough design challenges. Contact your TI representative to set up a meeting during the show.

Space Tech Webinar Series (March)
Get a deep dive on technical content reflecting some of the most commonly asked questions in the space market. Topics include:

• Optimizing your space design with the newest devices in TI’s rad hard portfolio
• Using fully differential amplifiers to optimize high speed signal chain interfaces
• Implementing demanding high current applications using Point of Load devices
• Understanding cosmic radiation effects on electronics and how to pick the right part

Radiation Handbook for Electronics (coming soon)
The Radiation Handbook for Electronics is your comprehensive guide to radiation effects for electronics. Building upon decades of knowledge from across TI’s expert teams, this 100+ page e-book features the latest design considerations for engineers who work on space, industrial and/or terrestrial applications. Readers from all design experience levels will:

• Learn about radiation environments, their effects on semiconductor devices and how to mitigate them
• Get an overview of radiation testing, procedures and requirements needed for radiation qualification
• Read about the benefits of using Texas Instruments’ portfolio of space grade integrated circuits
• And much more...

Aerospace & Defense Training Series (live now)
The Aerospace and Defense Training Series is your one-stop portal for product specific and system applications training material. Learn about the latest solutions to help you simplify designs, improve performance and meet stringent project requirements.
Thank you!