Linear OPAMP Characterization: Offset Voltage

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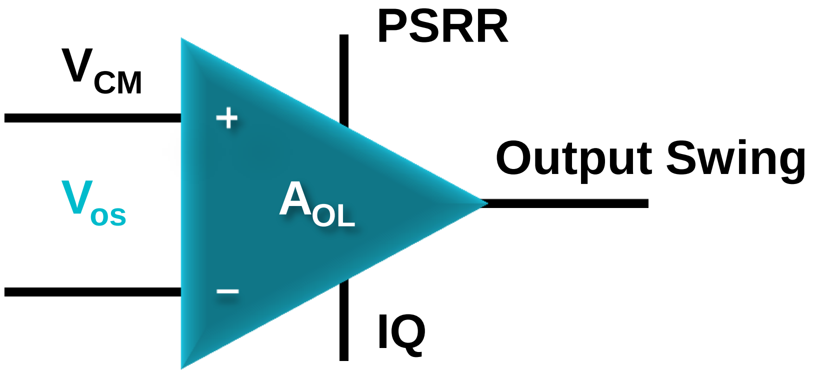
OPAMP verification

OPAMP Electrical Characterization:

- Characterizing the electrical behavior of an integrated circuit is critical during application troubleshooting
  - Non-conformances can be identified by comprehending device level characteristics in addition to system performance

- OPAMP electrical characterization series will review following topics:
  - **Voltage offset (V_{OS})**
  - V_{CM} / Common mode rejection ratio (CMRR)
  - Power supply rejection ratio (PSRR)
  - Output swing
  - Quiescent current
  - Open loop gain (A_{OL})



Prerequisites

Electrical characterization: VOS

- Common mode rejection ratio measurements methods are reviewed
- Following prerequisites are recommended prior to proceeding though the handbook

Prerequisites:

TI-Precision Labs (TIPL) courses:

VOS: TIPL - Op Amps: Vos and IB

ti.com/training-opamps-vos

Pocket Reference:

Training: Analog Engineer's Pocket Reference

ti.com/analogrefguide

Application handbook:

A-B-A: Board Level Troubleshooting

ti.com/board-level-troubleshooting

Simulation tools:

Simulations are presented within the handbook. It is recommended to install TINA-TI

TINA-TI can be downloaded for free on ti.com: http://www.ti.com/tool/tina-ti

OPAMP test loops

Overview:

- Analyzing datasheet parameters may appear a daunting task!
- Multiple parameters can be derived easily from offset (V_{OS}).
  - PSRR, CMRR, and AOL can be calculated by monitoring shifts

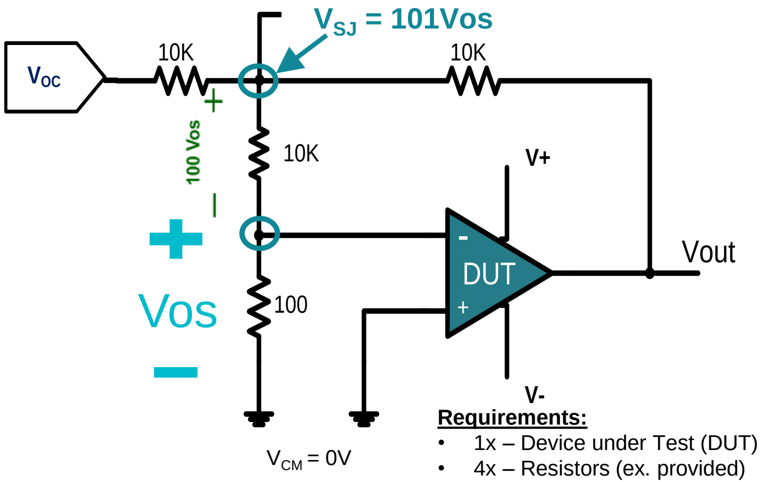
False Summing Junction (FSJ):

- Accurate VOS measurements can be obtained through test loops
  - **Benefits:**
    - Simplistic
    - Stable
    - Small
  - **Disadvantages:**
    - Feedback resistor load in parallel with other added loads
    - Loop drive function of DUT V_{OS}
- Majority of **DC** parameters determined with 4 resistors!

Measuring VOS:

- **VOS:** differential input voltage required to force output to mid-supply
  - best measured at the summing junction **(V_{SJ})**
- **Output control voltage (VOC):** Calibrate the out voltage to zero volts
  - Know as offset correction factor (derived from Kirchhoff's Voltage Law):

$$V_{OC} = -(V_{OUT} + VOS(302)) + 2VCM$$



Requirements:

- 1x – Device under Test (DUT)
- 4x – Resistors (ex. provided)
  - Resistor values can be varied depending on device

Example:

- V+ = +10V
- V- = -10V
- V_{OUT} = 0V
- V_{OC} = 0V (ideal opamp)

Results:

- V_{SJ}= 1.01mV
- 1.01mV = (101)Vos = V_{SJ}

  10µV = Vos

False summing junction

Simulation Overview:

- TINA-TI can be utilized to simulate a false summing junction circuit
  - **Figure 1 example**: OPA192
  - A reference design downloaded through TI.com
    - Link: http://www.ti.com/product/OPA192/technicaldocuments

- Review the TI datasheet prior to completing simulations
  - Verify: Supply range, VCM range and remaining parameters.

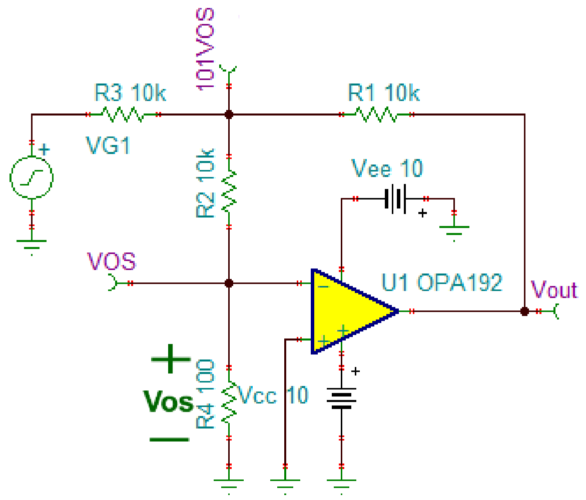


Figure: Representative circuit diagram created in TINA-TI.

Note: Device variation within datasheet limits may not be reflected in simulations

Datasheet offset voltage

VOS test conditions are provided within the TI product datasheet

- **Ensure** V_{OUT} approximately equal to mid-supply
- **Note:** High speed amplifiers measurements may require a solder down solution

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = +8 V to +36 V)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	μV
V_{OS}	Input offset voltage	T_A = 0°C to 85°C			±8	±50	μV
V_{OS}	Input offset voltage	T_A = –40°C to +125°C			±10	±75	μV
V_{OS}	Input offset voltage	V_{CM} = (V+) – 1.5 V			±10	±40	μV
V_{OS}	Input offset voltage	V_{CM} = (V+) – 1.5 V	T_A = 0°C to 85°C		±25	±150	μV
V_{OS}	Input offset voltage	V_{CM} = (V+) – 1.5 V	T_A = –40°C to +125°C		±50	±250	μV

http://www.ti.com/lit/ds/symlink/opa192.pdf