Simplify and Optimize Your Design with Logic and Level Shifters

Standard Logic and Translation
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Agenda: Simplify and Optimize Your Design with Logic and Level Shifters

- Overview of Standard Logic Portfolio
- Understanding CMOS circuits
- Common Applications Questions
- Simple system solutions
  - Use Cases for Logic and Level Translators
  - Building Blocks examples
- Open Forum for QA/Feedback/Suggestions
# Standard Logic – Overview

## Voltage Translation
- **Product families**
  - Direction controlled
  - Auto direction
  - Application specific
  - Translating gates

## Gates Buffers
- **Product families**
  - Gates
  - Buffers
  - Drivers

## Multi-gates FFLR
- **Product families**
  - Multi-gates*
  - Buffers
  - Flip flop & Latches
  - Shift registers

## Specialty Logic
- **Product families**
  - Configurable, Combo Logic
  - Logic comparators, Counters
  - Monostable multivibrators
  - Misc (Terminators, Adders, Timers)

## Transceivers Encoders Decoders
- **Product families**
  - Transceivers
  - Encoders
  - Decoders

## Sectors/EEs
- **HEV/EV**
- **ADAS**
- **Infotainment**
- **Motor Drive**
- **Sensor Fusion**
- **Surround sound**
- **Industrial Automation**
- **Test and Measurement**
- **Body Electronics**
- **Cluster**
- **Building Automation**
- **Factories, Servers, Grid**
- **HEV/EV**
- **ADAS**
- **Infotainment**
- **Motor Drive**

## Popular Devices
- **SN74AXC8T245**
  - 8 bit, 0.65V-3.6V Translator
- **LSF0204-Q1**
  - 4-bit, 0.9V-5.5V Translator
- **TXS0104E-Q1**
  - 4-bit bidirectional translator
- **SN74LVC1G17-Q1**
  - 1-bit Schmitt Trigger Buffer
- **SN74AUP1G08**
  - Low Power Single AND Gate
- **SN74LVC1G00-Q1**
  - Single channel NAND gate
- **SN74LV125A-Q1**
  - 4-bit Buffer with Enable
- **SN74HC21-Q1**
  - Dual 4-Input AND Gate
- **SN74AHC595-Q1**
  - 8-bit Shift Register w/enable
- **SN74HC193-Q1**
  - 4-bit Synchronous Counter
- **SN74LV123A-Q1**
  - Retriggerable One-shot
- **SN74HC4060-Q1**
  - Oscillator + 14-bit Counter
- **SN74AHC245-Q1**
  - 8-bit Bus Transceiver w/Enable
- **SN74HC253**
  - Dual 4 to 1 Encoder w/Enable
- **SN74HC138-Q1**
  - Single 3 to 8 Decoder/Demux
CMOS Input Characteristics

Shoot-through Current

TI Information-Selective Disclosure
Logic Use Case: Combining Power Good Signals

Power Good with AND Gate

- **DC-DC**: Active High Power Good
- **AND**: Active High Enable
- **Processor**: Active High Enable

**What problem it solves?**
- Identifying power good status of the system, where multiple DC-DCs are used. AND is used when the output of the DC-DC is active high as well as the enable input of the processor is active high.

**Popular Products**
- SN74LVC1G08 | SN74HC21A-Q1

Power Good Options

- **DC-DC**: Active High Power Good
- **NAND**: Active Low Enable
- **Processor**: Active High

**What problem it solves?**
- Identifying power good status of the system, where multiple DC-DCs are used.

<table>
<thead>
<tr>
<th>Gates</th>
<th>Power Good Input</th>
<th>Enable Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOR</td>
<td>Active Low</td>
<td>Active High</td>
</tr>
<tr>
<td>NAND</td>
<td>Active High</td>
<td>Active Low</td>
</tr>
<tr>
<td>AND</td>
<td>Active High</td>
<td>Active High</td>
</tr>
<tr>
<td>OR</td>
<td>Active Low</td>
<td>Active Low</td>
</tr>
</tbody>
</table>

Signal Enable using AND Gate

- **Tx Signal 1**
- **AND**: Enable
- **Tx Signal 2**

**What problem it solves?**
- AND gates can be used to gate signals. The second inputs can be used to force the output low or allow a signal to be transmitted.

**Popular Products**
- SN74LVC2G08 | SN74ALVC08A-Q1

TI Information-Selective Disclosure
Logic Use Case: Aggregating Error Signals

Enable a Switch Enable upon Error

What problem it solves?
- Combining error signals to enable a switch.

Popular Products
- SN74AHC1G32 | SN74LVC32A-Q1

Reset MCU upon Error using OR

What problem it solves?
- Activates MCU reset when an error occurs.

Popular Products
- SN74AHC1G32 | SN74LVC32A-Q1

Activate Buzzer Upon Error using OR

What problem it solves?
- Combining error signals to turn on a buzzer.

Popular Products
- SN74AHC1G32-Q1 | SN74LVC1G32
## Logic Use Case: XOR Gate

### Phase Comparator using XOR

- **Phase Locked Loop/Clock Alignment**

What problem it solves? Commonly used in communications, an XOR gate can be used to convert the phase difference to a PWM signal.

Popular Products
- SN74LVC1G86
- SN74AUC1G86

### Single Ended to Differential signal

What problem it solves? Dual XOR gate can be used to convert the single ended signal to differential signal with low skew.

Popular Products
- SN74LVC2G86
- SN74AUC2G86
What happens if $V_I > V_{CC}$?

* Positive sign indicates sinking current, negative current indicates sourcing current.

### 6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>$-0.5$</td>
<td>$6.5$</td>
<td>V</td>
</tr>
<tr>
<td>$V_I$</td>
<td>$-0.5$</td>
<td>$6.5$</td>
<td>V</td>
</tr>
<tr>
<td>$V_O$</td>
<td>$-0.5$</td>
<td>$6.5$</td>
<td>V</td>
</tr>
</tbody>
</table>

* Positive sign indicates sinking current, negative current indicates sourcing current.
Partial Power Down

- **Bias $V_{CC}$**
- **Power-Up 3-State**
- **$I_{OFF}$**
  - L3 – Live Insertion
  - L2 – Hot Insertion
  - L1 – Partial Power Down

**Electrical Isolation**

- **Allows voltage on Input/output when $V_{CC} = 0$**
- **Prevents input/output signal inversion during power-up or power-down**

**6.5 Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>$-40^\circ C$ to $85^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_I$ or $V_O$ = 5.5 V</td>
<td>0</td>
<td>$\pm 10$</td>
</tr>
</tbody>
</table>

**Families Supporting Partial Power Down ($I_{OFF}$)**

- ABT, ALVT, AVC, AUC, AUP, GTL, GTLP, LV-A, LVC, LVT, VME
What do I do with unused inputs?
Floating logic inputs tend to drift to the logic threshold region and cause excessive current draw from $V_{CC}$, in addition to oscillation.

**Bus Hold**

**Problem**
Floating logic inputs tend to drift to the logic threshold region and cause excessive current draw from $V_{CC}$, in addition to oscillation.

**Solution**
Bus-hold circuitry pulls the logic input to its last known state.

**Value**
Pullup and pulldown resistors are no longer required or recommended. Inputs will not float to unstable levels.
Unused Inputs – What do I do

Utilizing NAND/NOR as Inverting Buffer

What problem it solves?
• Utilizing a NAND gate as an inverter when spare gates are available in multi input gates. In this case, the desired signal needs to be inverted for further comparison.

Popular Products
• SN74AHC1G00-Q1 | SN74AHC00-Q1

Utilizing OR/AND as a Buffer

What problem it solves?
• Utilizing an OR gate as a buffer when spare gates are available in multi input gates. In this case the buffer is being used as a delay between the shift registers.

Popular Products
• SN74AHC1G32-Q1 | SN74LVC32A-Q1
What happens when the inputs has slow rise time?

**Bad Circuits**

SN74LVC1G175
D-Type Flip-Flop

**Oscillations**

Slow Rising Edge input results in output oscillations (Inverter)

**Excessive Current**

\[ \frac{1}{2} V_{CC} \]

\[ I_{CC} \]
Schmitt-Trigger Overview

TI Information-Selective Disclosure
**Logic Use Case: Correcting Slow, Noisy Inputs**

**Increase Edge Rate w/Schmitt Trigger**

- **What problem it solves?**
  - Creates a sharp rising edge for slow rising or noisy input signals to eliminate on/off timing discrepancy.

- **Popular Products**
  - SN74LVC1G17-Q1 | SN74LVC2G17

**Mechanical Push Button Debounce**

- **What problem it solves?**
  - Creates a single sharp pulse instead of a series of pulses which could trigger the output multiple times on a single button press.

- **Popular Products**
  - SN74LVC14A | SN74LVC2G17-Q1
Logic use case: Adding a time delay

**Time Delay using Schmitt Trigger**

What problem it solves?
- The RC circuit creates a time delay that can be specified by the user that is then fed into the buffer, returning the pulse of the delay at the output.

Popular Products
- SN74LVC1G17-Q1 | SN74LVC2G17

**Rising Edge Time Delay using Schmitt Trigger Buffer**

What problem it solves?
- The shown diode added to the RC circuit will allow falling edges to bypass the delay

Popular Products
- SN74LVC1G17-Q1 | SN74LVC3G17

**Falling Edge Time Delay using Schmitt Trigger Buffer**

What problem it solves?
- The shown diode added to the RC circuit will allow rising edges to bypass the delay

Popular Products
- SN74LVC1G17-Q1 | SN74LVC2G14

TI Information-Selective Disclosure
Do we have gates with Schmitt-trigger inputs?

SN74LVC1G97-Q1

**LOGIC FUNCTION**
- 2-to-1 data selector
- 2-input AND gate
- 2-input OR gate with one inverted input
- 2-input NAND gate with one inverted input
- 2-input AND gate with one inverted input
- 2-input NOR gate with one inverted input
- 2-input OR gate
- Inverter
- Noninverted buffer

SN74AUP1G99

<table>
<thead>
<tr>
<th>PRIMARY FUNCTION</th>
<th>COMPLEMENTARY FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-state buffer</td>
<td>3-state inverter</td>
</tr>
<tr>
<td>3-state inverter</td>
<td>3-state 2-to-1 data selector MUX, inverted out</td>
</tr>
<tr>
<td>3-state 2-to-1 data selector MUX, inverted out</td>
<td>3-state 2-input AND</td>
</tr>
<tr>
<td>3-state 2-input AND</td>
<td>3-state 2-input AND, 1 input inverted</td>
</tr>
<tr>
<td>3-state 2-input NAND</td>
<td>3-state 2-input NOR, both inputs inverted</td>
</tr>
<tr>
<td>3-state 2-to-1 NAND,</td>
<td>3-state 2-input NAND, both inputs inverted</td>
</tr>
<tr>
<td>3-state 2-input XOR</td>
<td>3-state 2-input NAND, both inputs inverted</td>
</tr>
<tr>
<td>3-state 2-to-1 XOR</td>
<td>3-state 2-input NAND, both inputs inverted</td>
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<td>3-state 2-input NAND, both inputs inverted</td>
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</tbody>
</table>

Configurable Gate

2-to-1 Data Selector

2-Input AND Gate
CMOS Output Characteristics

- Nearly Constant Resistance
- Ideal Constant Resistance

- $V_{OL}(\text{max})$
- Max FET Current @ $V_{CC}$
- $V_{OL}(\text{typ})$

- $I_{OL}$ vs. $V_{OL}$
- $I_{SC}$ vs. $V_{OL}$

TI Information-Selective Disclosure
Logic use case: Increasing drive strength

Peripheral driver requiring higher current

What problem it solves?
• Used to increase drive strength between the processor and a peripheral devices. (ex. LED)

Popular Products
• SN74LVC1G07 (Open Drain)
• SN74LV125A-Q1

Parallel Outputs for High Current Drive

What problem it solves?
• When putting two components in parallel their current will add, thus increasing the current drive.

Popular Products
• SN74LVC125A-Q1

*Timing issues can occur if done with buffers from different packages
# Logic use case: Improving signal quality

## Buffer for long traces

- **What problem it solves?**
  - Used to drive high capacitance lines or long traces.

- **Popular Products**
  - SN74LVC1G17 | SN74LV125A-Q1

## Fan Out using Octal Buffer

- **What problem it solves?**
  - Increases current drive from CPU to multiple peripherals
  - Distribute load capacitance

- **Popular Products**
  - SN74AHC244A | SN74LVC244A-Q1

## Unidirectional Switch using 3-State Buffer

- **What problem it solves?**
  - Allows for signal to pass when enabled.

- **Popular Products**
  - SN74LVC1G125-Q1 | SN74AUP1G125

## Bidirectional communication using Transceiver

- **What problem it solves?**
  - Allows for bidirectional communication between a master and slave device while keeping signal integrity.

- **Popular Products**
  - SN74AHC245-Q1

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**TI Information-Selective Disclosure**
### Up/Down Translation using Open Drain Buffer

<table>
<thead>
<tr>
<th>FPGA 1.8V</th>
<th>→</th>
<th>MCU</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS₁=3.3V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**What problem it solves?**
- Utilized as flexible voltage translation from a processor to an external peripheral

**Popular Products**
- SN74LVC1G07 | SN74LVC07A-Q1

### Voltage Source Separation using Open Drain Buffer

<table>
<thead>
<tr>
<th>Controller</th>
<th>→</th>
<th>MCU</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS₁=3.3V from Battery</td>
<td>VS₂=3.3V from system rail</td>
<td></td>
</tr>
</tbody>
</table>

**What problem it solves?**
- Used to separate two voltage domains

**Popular Products**
- SN74LVC1G07-Q1 | SN74LVC07A

### Wired-AND/OR logic using Open Drain buffer

<table>
<thead>
<tr>
<th>FPGA 1.8V</th>
<th>→</th>
<th>MCU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vx=3.3V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**What problem it solves?**
- One chip solution to integrate Logic-AND function & signal translation using OD buffer (also termed as Wired-AND)

**Popular Products**
- SN74LVC1G07 | SN74LVC07A
CMOS power consumption

Total Power Consumption

\[ P_{\text{TOTAL}} = P_S + P_T + P_{\text{LC}} + P_{\text{LR}} \]

- **Static Power Consumption** \((P_S)\)
  \[ P_S = V_{CC} I_{CC\text{(max)}} \]

- **Resistive Load Power Consumption** \((P_{LR})\)
  \[ P_{LR} = \sum \left[ D_n \left( V_{CC} - V_{OHn} \right) \left( V_{OHn} / R_{Ln} \right) \right] \]

- **Dynamic Power Consumption**
  - **Transient Power Consumption** \((P_T)\)
    \[ P_T = C_{pd} V_{CC}^2 f_i N_{SW} \]
  - **Capacitive Load Power Consumption** \((P_{LC})\)
    \[ P_{LC} = \sum \left[ C_{Ln} f_{On} \right] V_{CC}^2 \]

\(V_{CC}\) := supply voltage
\(I_{CC\text{(max)}}\) := max static supply current (from datasheet)
\(C_{pd}\) := dynamic power-dissipation capacitance (from datasheet)
\(f_i\) := input frequency
\(N_{SW}\) := number of inputs switching
\(C_{Ln}\) := Load capacitance at each output, 1 through n
\(f_{On}\) := Output frequency at each output, 1 through n
\(D_n\) := Duty cycle of output
\(V_{OHn}\) := Output high voltage @ load current (from datasheet)
Understanding Thermal Values

\[ \Delta T = P_{TOTAL} R_{\theta JA} \]

Example

\[ \Delta T = 100\text{mW} \times 177.4 \, ^\circ\text{C/W} \]

\[ \Delta T = 17.7 \, ^\circ\text{C} \]

If operating at 125°C, the junction would increase to

\[ 125 + 17.7 = 142.7 \, ^\circ\text{C} \]

* The majority of logic devices will never hit the maximum junction temperature if operated within the datasheet limits. \( R_{\theta JA} \) is the most commonly required thermal value.
Logic Use Case: Output expansion with limited I/Os

### MCU to Multiple Indicator LED’s using a Shift Register

**What problem it solves?**
- Used to expand the MCU’s number of outputs for individual LED control

**Popular Products**
- SN74AHC595-Q1 | SN74HC595

### Driving Stepper Motor w/Shift Register

**What problem it solves?**
- Used to expand the MCU’s number of outputs for stepper motor control

**Popular Products**
- CD4021B-Q1 | SN74HC595

### 7-Segment Display using Shift Register

**What problem it solves?**
- Used to expand the MCU’s number of outputs for 7 segment displays

**Popular Products**
- SN74AHC595-Q1 | CD4021B
Design Challenges

Building a design that can drive an LED Matrix or 7-segment display in a space-constrained environment and a limited number of outputs

Solution / Value

- Subsystem Adaptable to a Wide Range of Space-Constrained Applications
- Only Three GPIO Pins Required to Drive Any Multiple of Eight Channels
- X1QFN smallest available logic packaging for high pin count devices
- Total Solution size fits within the board area of a single 7 segment display

Blog: The next-generation QFN: Do you have what it takes to use it?

TIDA-01233
Logic Use Case: Clock division and Flip-Flop

Clock Division using D-Flip Flop

- What problem it solves?
  - Used when a user wants to decrease clock frequency

- Popular Products
  - SN74LVC1G374 | SN74AHC74Q-Q1

Multiple Clock Divisions using counter

- What problem it solves?
  - Utilized when a 2^n clock division is required
  - For example, a 4 bit counter can do a 16x clock division

- Popular Products
  - SN74HC163-Q1 | SN74HC193

Buck converter control using SR Flip Flop

- What problem it solves?
  - Synchronous buck controller using SR flip flop
  - Controlled timing of Pass FET and reverse current FET

- Popular Products
  - SN74AUP1G74 | SN74LVC2G74

TI Information-Selective Disclosure
Translation by Interface: Serial Peripheral Interface (SPI)

Does your system have a SPI interface to a peripheral such as:

- Bluetooth Low Energy Module
- GPS Module
- WiFi Module
- Sensors (Image, Temp, Pressure, etc.)
- Accelerometer
- Memory

**Why:** Simultaneous Individually Addressable Communication between central processor and peripheral

**Key Careabouts:**
- Push-Pull Architecture
- 4 Individual Channel Direction Control
- Low Current Consumption

**Recommendation:**
- TXB0104-Q1
- SN74AXC4T774-Q1*

**Data Rate → 200 Mbps**
- Bit Count → 3 or 4
- Voltage → 1.8 to 3.3V
Direction Controlled Translation Use-Cases
Audio Encoding with Inter-IC Sound (I²S) or Pulse-Code Modulation (PCM)

Does your system have an audio codec ADC or DAC communicating over I²S or PCM with a CPU or DSP?

Why: Bidirectional Support and Signal Redriving with Translation

Key Careabouts:
- Push-Pull Architecture
- 2 by 2 Channel Direction Control
- Bit Count → 3 to 4
- Data Rate → 48 Mbps
- Voltage → 1.8 to 3.3V

Recommendation:
- SN74AVC4T245-Q1
- SN74AXC4T245-Q1

Does your I²S or PCM signaling require individual channel control?

Why: Bidirectional Support with individual channel control

Key Careabouts:
- Push-Pull Architecture
- 4 Individual Channel Direction Control
- Bit Count → 4
- Data Rate → 48 Mbps
- Voltage → 1.8 to 3.3V

Recommendation:
- TXB0104-Q1
- SN74AXC4T774-Q1
Direction Controlled Translation Use-Cases
Peripheral Interface with Universal Asynchronous Receiver-Transmitter (UART)

Does your system have a UART interface to a peripheral such as:
- Bluetooth Low Energy Module
- GPS Module
- Sensors (Image, Temp, Pressure, etc.)
- Memory
- Secondary Microcontroller
- USB to UART Bridge

Why: Simultaneous Bidirectional Communication between central processor and peripheral

Key Careabouts:
- Push-Pull Architecture
- 2 by 2 Channel Direction Control
- Low Current Consumption
- Bit Count → 4
- Data Rate → 20 Mbps
- Voltage → 1.8 to 3.3V

Recommendation:
SN74AVC4T245
SN74AXC4T245-Q1

Stage 1 Stage 2 Stage 3 Stage 4 Stage 5 FCS Ready
Does your system utilize JTAG to provide in-system programming or debug?

**Why:** Simultaneous Individually Addressable Communication with Translation

---

Does your debug port run on a reduced pin count JTAG with only 2 pins?

**Why:** Unidirectional Translation and Redriving

---

**Key Careabouts:**
- Push-Pull Architecture
- **4 Individual Channel Direction Control**
- Bit Count → 4
- Data Rate → 200 Mbps
- Voltage → 1.8 to 3.3V

**Recommendation:**
- SN74AVC4T774
- SN74AXC4T774-Q1

---

**Key Careabouts:**
- Push-Pull Architecture
- **2 Bit Unidirectional**
- Bit Count → 2
- Data Rate → 200 Mbps
- Voltage → 1.8 to 3.3V

**Recommendation:**
- SN74AVC2T45
- SN74AXC1T45
**Unidirectional translation: 2N7001T**

### Discrete FET replacement with Unidirectional level shifter

What problem it solves?
- Replace discrete FETs using TI's unidirectional translation gates

**Popular Products**
- 2N7001T-Q1 | SN74AUP1T34-Q1

### LED driving using Unidirectional level shifter

What problem it solves?
- Drive a LED indicator using unidirectional translation

**Popular Products**
- 2N7001T-Q1 | SN74AUP1T34-Q1 | SN74LV1T34
What problem it solves?
- Activates a reset when thermal sensor error occurs or system reset input sent to processor

Popular Products
- SN74AHC1G32-Q1 | SN74LVC32A-Q1

What problem it solves?
- Identifies power good status of the system, where multiple DC-DCs are used. Low cost method of system power good implementation instead of using processor GPIOs for individual power good signals.

Popular Products
- SN74LVC1G08-Q1 | SN74HC21A-Q1
What problem it solves?
• Translates I²C / I2S communication signals between processor and peripherals (Audio DSP / CMOS sensor) which are at different IO voltage levels (3.3V to 1.8V).

Popular Products
• TXB0104-Q1 | TXS0102-Q1 | LSF0102-Q1

What problem it solves?
• Activates a reset when thermal sensor error occurs or system reset input sent to processor

Popular Products
• SN74AHC1G32-Q1 | SN74LVC32A-Q1

What problem it solves?
• Identifies power good status of the system, where multiple DC-DCs are used. Low cost method of system power good implementation instead of using processor GPIOs for individual power good signals.

Popular Products
• SN74LVC1G08-Q1 | SN74HC21A-Q1

What problem it solves?
• Used to increase drive strength between the processor and indicator LED

Popular Products
• SN74LVC1G125-Q1 | SN74AHCT1G125-Q1
Selecting the Right Voltage Level Translator for Common Interfaces
## Quick Select for Translation Devices

### Select by Interface

<table>
<thead>
<tr>
<th>Interface</th>
<th>2 Ch</th>
<th>4 Ch</th>
<th>6 Ch</th>
<th>8 Ch</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI</td>
<td>--</td>
<td>AVC4T774 TXB0104</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>UART</td>
<td>--</td>
<td>AVC4T774 TXB0104</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>JTAG</td>
<td>--</td>
<td>AVC4T774 TXB0104</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>I2S</td>
<td>--</td>
<td>TXB0104 AVC4T245</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>I2C</td>
<td>TXS0102 LSF0102</td>
<td>TXS0104E LSF0204</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>MDIO</td>
<td>TXS0102 LSF0102</td>
<td>TXS0104E LSF0204</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>SMBus</td>
<td>TXS0102 LSF0102</td>
<td>TXS0104E LSF0204</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>RMI/FGMII</td>
<td>--</td>
<td>TXB0106</td>
<td></td>
<td>AXC8T245</td>
</tr>
<tr>
<td>Quad-SPI</td>
<td>--</td>
<td>TXB0106</td>
<td>TXB0108</td>
<td></td>
</tr>
<tr>
<td>SDIO</td>
<td>--</td>
<td>TXS0206 TXS0206-29</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>IC-USB</td>
<td>--</td>
<td>AVC2T8T2 TXS0202</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>SD/MMC</td>
<td>--</td>
<td>TXS0206 TXS0206-29</td>
<td>--</td>
<td></td>
</tr>
</tbody>
</table>

### Select by Translation and Supply Configuration

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Supply</th>
<th>1 Ch</th>
<th>2 Ch</th>
<th>4 Ch</th>
<th>8 Ch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto Bidirectional (Dual Supply)</td>
<td>1.65 – 5.5V</td>
<td>TXS0101</td>
<td>TXS0102</td>
<td>TXS0104E</td>
<td>TXS0108E (1.2 – 5.5V)</td>
</tr>
<tr>
<td></td>
<td>1.2 – 5.5V</td>
<td>TXB0101</td>
<td>TXB0102</td>
<td>TXB0104</td>
<td>TXB0108</td>
</tr>
<tr>
<td></td>
<td>0.95 – 5.5V</td>
<td>LSF0101</td>
<td>LSF0102</td>
<td>LSF0204</td>
<td>LSF0108</td>
</tr>
<tr>
<td>Direction Controlled (Dual Supply)</td>
<td>0.65-3.6</td>
<td>AXC1T45</td>
<td>--</td>
<td>--</td>
<td>AXC8T245</td>
</tr>
<tr>
<td></td>
<td>1.2-3.6</td>
<td>AXC1T45</td>
<td>AVC2T45</td>
<td>AVC4T245</td>
<td>AXC8T245</td>
</tr>
<tr>
<td></td>
<td>1.65-5.5</td>
<td>LVC1T45</td>
<td>LVC2T45</td>
<td>--</td>
<td>LVC8T245</td>
</tr>
<tr>
<td>Unidirectional</td>
<td>1.65-5.5V</td>
<td>LV1T125</td>
<td>--</td>
<td>LV4T125</td>
<td>--</td>
</tr>
<tr>
<td>Dual Supply</td>
<td>0.65 – 3.6V</td>
<td>AXC1T45</td>
<td>AVC2T244 (0.9 - 3.6V)</td>
<td>AVC4T234 (0.9 - 3.6)</td>
<td>AXC8T245</td>
</tr>
<tr>
<td>Translating Gates AND, OR, NOR... (Single Supply)</td>
<td>2.3-3.6</td>
<td>SN74AUP1T Family</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td>1.65-5.5V</td>
<td>SN74LV1T Family</td>
<td>--</td>
<td>LV4T125</td>
<td>--</td>
</tr>
</tbody>
</table>
## Auto-Bidirectional Translators

<table>
<thead>
<tr>
<th>Metrics</th>
<th>TXB</th>
<th>TXS</th>
<th>LSF</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Drive strength</strong></td>
<td>Very low drive of 20ua due to 4K buffer</td>
<td>Passive translation with NMOS; no drive</td>
<td>Passive translation with NMOS; no drive</td>
</tr>
<tr>
<td><strong>Applications/ Interface</strong></td>
<td>Mostly suitable for push-pull applications</td>
<td>Suitable for open drain applications</td>
<td>Push pull and open drain applications</td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>Up to 140Mbps</td>
<td>Up to 24Mbps</td>
<td>High speed up to 200Mbps</td>
</tr>
<tr>
<td><strong>Translation flexibility</strong></td>
<td>Buffered; Fixed translation</td>
<td>Integrated 10k resistors-reduces BOM cost of the system; but inflexible</td>
<td>Flexible translation due to external resistors</td>
</tr>
<tr>
<td><strong>I/O ports</strong></td>
<td>Referenced to Vcca or Vccb</td>
<td>Referenced to Vcca or Vccb</td>
<td>Multi-voltage translation in single device</td>
</tr>
<tr>
<td><strong>Edge- acceleration</strong></td>
<td>Integrated one-shot</td>
<td>Integrated one-shot</td>
<td>No integrated one-shot</td>
</tr>
<tr>
<td><strong>Vih/Vil requirements</strong></td>
<td>Datasheet spec has Vih/Vil</td>
<td>D/S has Vih/Vil spec, no Ron for the FET</td>
<td>No Vih / Vil conditions, has Ron spec</td>
</tr>
<tr>
<td><strong>Additional care-about</strong></td>
<td>Vcc&lt;=Vccb</td>
<td>Vcca&lt;=Vccb</td>
<td>Vccb&gt;Vcca+0.8</td>
</tr>
</tbody>
</table>

**Driver strength**

Very low drive of 20ua due to 4K buffer provides a passive translation with NMOS; no drive.

**Applications/ Interface**

Mostly suitable for push-pull applications.

**Speed**

Up to 140Mbps for TXB, up to 24Mbps for TXS, and high speed up to 200Mbps for LSF.

**Translation flexibility**

Buffered; Fixed translation for TXB, integrated 10k resistors reduces BOM cost of the system; but inflexible for TXS.

**I/O ports**

Referenced to Vcca or Vccb for both TXB and TXS, and multi-voltage translation in single device for LSF.

**Edge- acceleration**

Integrated one-shot for TXB and TXS, no integrated one-shot for LSF.

**Vih/Vil requirements**

Datasheet spec has Vih/Vil for TXB, D/S has Vih/Vil spec, no Ron for the FET for TXS, and no Vih / Vil conditions, has Ron spec for LSF.

**Additional care-about**

Vcc<=Vccb for TXB, Vcca<=Vccb for TXS, and Vccb>Vcca+0.8 for LSF.
Voltage level translator product portfolio

**Unidirectional**
- 1-,2-,4-bit
- Level translating
- Fast translation (190Mhz)
- Low Power (1mA)

**Specific application**
- Sensor I/F
- LV chipset IO
- PC/Compute Control IO

**Hero Parts**
- 2N7001T
- SN74AUP1T34
- SN74AVC4T234
- SN74AVC2T244

**Direction controlled**
- 1-,2-,4-,6-, 8-, 16-, 24-,32-bit
- Level translating
- High Speed (190Mhz)
- Push-pull Ios
- Low Power (60uA)

**Specific application**
- SPI, UART
- I2S
- IC-USB
- JTAG
- RGMII

**Hero Parts**
- SN74LVC8T245
- SN74AXC8T245
- SN74AXC1T45
- SN74AVC4T774

**Auto-Direction sensing**
- 1-,2-,4-,6-,8-bit
- Level translating
- High Speed 100Mhz
- Push-pull Ios, Open-drain Ios
- Most versatile solutions

**Specific application**
- SD Card
- SIM Card
- IC-USB

**Hero Parts**
- TXS0102
- TXB0304
- TXB0108
- LSF0108

**Translation + Logic Gates**
- 1-, 4-bit
- Level translating
- Perform Logic function + Translation
- Fast Operation (190Mhz)
- Low Power (1mA)

**Specific application**
- Chipset logic
- Control logics for compute
- Control logic for comms

**Hero Parts**
- SN74LV1T00
- SN74AUP1T08
- SN74LV1T34
- SN74AUP1T57
Backup: Logic Special Features
Floating logic inputs tend to drift to the logic threshold region and cause excessive current draw from $V_{CC}$, in addition to oscillation.

**Problem**

**Solution**

*Bus-hold* circuitry pulls the logic input to its last known state.

**Value**

Pullup and pulldown resistors are no longer required or recommended. Inputs will not float to unstable levels.
**Problem**

Signal integrity issues due to noise on edges at output

**Solution**

*Series damping resistors* slow edges and provide better impedance matching and line termination

**Value**

Eliminates the need for external series resistors

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RLC current impulse response

https://en.wikipedia.org/wiki/RLC_circuit

TI Information-Selective Disclosure
Partial Power Down

L3 – Live Insertion
L2 – Hot Insertion
L1 – Partial Power Down

Electrical Isolation

- Allows voltage on output when $V_{cc} = 0$
- Prevents unexpected device behavior during power-up or power-down
- Prevents signals from sourcing current through parasitic diodes
- Allows for power down of partial circuits within a system
- $I_{OFF}$ spec is required for partial power down operations
- Explanation of IOFF and the three levels of electrical protection

Families Supporting Partial Power Down ($I_{off}$)

ABT, ALVT, AVC, AUC, AUP, GTL, GTLP, LV-A, LVC, LVT, VME
Hot Insertion

- Problem: Outputs sometimes “follow” VCC at low voltages as VCC ramps
- Power-Up 3-State (PU3S) prevents this “following” until VCC reaches a trip point.
- Prevents bus to be loaded down upon power-up
- I_{OFF} and PU3S specs required for hot insertion
- PU3S App Note

**Example Circuit Implementation**

**Families Supporting Hot Insertion (I_{OFF} and Power-up 3-state)**

| ABT, ALVT, GTLP, LVCZ, LVT, VME |
Live Insertion

**Bias $V_{CC}$**

- **L3** – Live Insertion
- **L2** – Hot Insertion
- **L1** – Partial Power Down

**Electrical Isolation**

- **BIAS $V_{CC}$** Prevents unwanted glitches at the I/O
- **IOFF, PU3S, and BIAS $V_{CC}$** required for Live Insertion
- Staggered pins require pre-charge functionality
- [Live Insertion App Note](#)

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**Families Supporting Live Insertion**

($I_{OFF}$, Power-up 3-state, and BIAS $V_{CC}$)

- ABTE, GTLP, FB, VME

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**Circuit Implementation**

**Pre-Charge Circuit**

- With pre-charge
- Without pre-charge

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**TI Information-Selective Disclosure**

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Logic Feature List †

- **Bus Hold – ABT, ALVC, ALVT, AVC, AUC, FCT, GTL, GTLP, LVC, LVT, VME**
  - Bus hold circuitry in selected logic families helps solve the problem of floating inputs and eliminates the need for pull-up or pull-down resistors by holding the last known state of the input. See \( I_{\text{HOLD}} \) or \( I_{\text{BLH}}, I_{\text{BHH}}, I_{\text{BLO}}, \) and \( I_{\text{BHHO}} \) on data sheet. The Bus Hold devices typically have an “H” in the part number.

- **Series Damping Resistors – ABT, ALVC, ALVT, F, GTLP, LVC, LVT, VME**
  - Series damping resistors limit signal overshoot and undershoot by providing better impedance matching and line termination without the need for external resistors.

- **Partial Power Down (Level 1 Isolation - \( I_{\text{off}} \)) – ABT, ALVT, AVC, AUC, AUP, CBTLV, CBT-C, GTL, GTLP LV-A, LVC, LVT, VME**
  - IOFF circuitry prevents the device from being damaged during hot insertion. See IOFF specifications on data sheet.

- **Hot Insertion (Level 2 Isolation – Ioff and Power-up 3-state) – ABT, ALVT, GTLP, LVCZ, LVT, VME**
  - Power-up 3-state ensures valid output levels during power up and valid Z on the outputs during power down. See IOZPU, IOZPD.

- **Live Insertion (Level 3 Isolation – Ioff, Power-up 3-state, and BIAS VCC) – GTLP, FB, CBT, CBTLV, VME**
  - Precharges I/O capacitance, preventing glitching of active data.

- **Mixed-Voltage-Tolerant I/Os and Level Shifting – AVC, ALVC, ALVT, AUC, AUP, GTL, GTLP, LV-A, LVC, LVT**
  - Systems use mixed supply voltages and TLL or CMOS levels in many designs. Most advanced-logic families allow mixed-signal interfacing and provide level-shifting functions for certain mixed-voltage applications.

- **JTAG – ABT, ACT, BCT, LVT**
  (†selected functions)
TI Design: Automotive-Qualified 16-Bit Rotary Quadrature Decoder

Design Challenges

Creating a simple front-end digital decoder for a quadrature encoder (rotary knob), while minimizing processing time from an MCU

Solution / Value

- I2C interface
- Works with any rotary quadrature encoder
- Overvoltage tolerant inputs allow for a wide variety of input voltage ranges
- Voltage translation allows for 2-V to 5-V logic outputs
- Open-drain interrupt output indicates to the MCU when a change has occurred
- Low power standby operation
- Frees up MCU operating time

Visit: [ti.com/tidesigns](http://ti.com/tidesigns)

Part number: TIDA-00580

Rotary decoder circuitry fits inside the red circle, behind the rotary knob