PCB Thermal Design with ultra small flip-chip packages (without Thermal Pad): HotRod

Arief Hernadi - Application Engineer CCP (APP, BSR)

With material provided by Frank De Stasi, Marc-Davis Marsh, Anthony Fagnani
Agenda

1. Thermal Design Primer
   • Goal Thermal Management
   • Thermal Design Terminology

2. Hot Rod Package
   • Benefit of Hot Rod Package
   • Comparing Hot-Rod and Standard Wirebond QFN Package

3. Designing a PCB for best Performance
   • Estimating Board Copper Size
   • Layout a Hot-Rod Package
   • Thermal Vias

4. Example of LMR33630 SOIC and Hot Rod Package
   • Evaluating Thermal performance of both package in a given design
Thermal Design Primer
Heat Transfer

IC Power Loss is **Heat**

- **Conduction** or diffusion: The transfer of energy between objects that are in physical contact
  - The primary path for heat leaving the IC package
- **Convection**: The transfer of energy between an object and its environment, due to fluid motion
  - The primary path for heat leaving the PCB
- **Radiation**: The transfer of energy to or from a body by means of the emission or absorption of electromagnetic radiation
  - The secondary path for heat leaving the PCB and the IC package

**Goal: provide minimum resistance path for heat flow**

» Minimum IC temp rise
Heat transfer basic theory

- **Conduction:**
  \[ Q = \frac{k \times A \times \Delta T}{L} \]

- **Convection:**
  \[ Q = h \times A \times \Delta T \]

- **Radiation:**
  \[ Q = \varepsilon \times \sigma \times A \times \left( T_b^4 - T_a^4 \right) \]

- Where:
  - Q = heat
  - k = material conductivity
  - A = area
  - L = thickness (length)
  - h = convection coefficient
  - \( \Delta T \) = temperature delta
  - \( \varepsilon \) = emissivity
  - \( \sigma \) = Stefan-Boltzmann constant

Dominant

Lateral and Perpendicular Conduction

Thermal vias

Convection

Radiation
Analogy Between Thermal and Electrical Resistance

**Electrical Resistor**

\[ V_1 \quad \underline{\text{V V V V V}} \quad V_2 \]

\[ I \quad \underline{\text{R}} \]

\[ R = \frac{(V_1 - V_2)}{I} \]

\[ I \times t = Q \]

**Thermal Resistor**

\[ T_1 \quad \underline{\text{V V V V V}} \quad T_2 \]

\[ P \quad \underline{\text{\(\theta\)}} \]

\[ \theta = \frac{(T_1 - T_2)}{P} \]

\[ P \times t = Q \]

Temperature -> “Thermal potential”
Power -> “Thermal current”
Heat -> “Electrical charge”

Electrical => Q is Charge

Thermal => Q is Heat
Typical Values

- $\theta_{\text{CU}} \approx 71.4^\circ\text{C/W}$
  - Based on 1oz copper, $W=1\text{cm}$, $L=1\text{cm}$. $\lambda_{\text{CU}} = 4 \text{ W/cm K}$

- $\theta_{\text{VIA}} \approx 261^\circ\text{C/W}$
  - Based on 0.5oz plating thickness, for 300um via (12mil)

- $\theta_{\text{FR4}} \approx 13.9^\circ\text{C/W}$
  - Based on 320um thickness, $W=1\text{cm}$, $L=1\text{cm}$. $\lambda_{\text{FR4}} = 0.0023 \text{ W/cm K}$

- $\theta_{\text{SA}} \approx 1000^\circ\text{C/W}$
  - $W=1\text{cm}$, $L=1\text{cm}$. $h = 0.001 \text{ W/cm K}$
Thermal Design Terminology

At each interface from the junction to the ambient air there is an associated thermal resistance.
The Goal of Thermal Management

Maximum junction temperature. Given in data sheet of converter; usually 125°C or 150°C

Power dissipation of converter. Depends on required output power and converter efficiency

Thermal resistance from ambient to junction of converter. Depends on everything; package, copper area, airflow, etc.

\[ T_J = T_A + P_D \cdot \theta_{JA} \]

Maximum ambient temperature. Specified by customer application

The goal is to keep \( T_J \) below the maximum specified in the data sheet.
Some Basic Terminology

- Thermal resistance; \( \theta_{JA} \)
  - Total thermal resistance from the junction to the ambient environment

- Not too easy to estimate, in some cases

- Depends on many factors
  - Package type
  - Copper heatsink area
  - Air flow
  - Number of copper planes
  - Weight of copper planes
  - Number of thermal vias
  - Adjacent components
  - Power dissipation
Some Basic Terminology

Difference between θ-type and Ψ-type Parameters

**θ Type**
- All the heat flows from the junction to location X
  - Assumes isothermal conditions
- Location X serves as the external heat sink to the package
  - Assumes non-isothermal conditions

**ψ Type**
- Only a fraction of the heat flows from the junction to location X
  - Assumes non-isothermal conditions
- Temperature gradient exists in location X
  - Assumes non-isothermal conditions
Power dissipation = 2 W

Pad

Chip

PWB

Cu Plate at constant temp = 25 °C

Junction temp monitor

Power is dissipated in all directions

\[ \Psi_{JT} = \frac{T_{Junc} - T_{case}}{\text{Power}} \]

Case temp monitor

Theta JC

All the Power is forced to be dissipated only in one direction {UPWARD}
Hot Rod (Flip Chip) Package
Comparing Hotrod Package and Wirebond Package

Minimize EMI through:
1. No-wirebond VSON packaging
2. Symmetric pinout
3. Spread spectrum feature
Package Differences

Exposed Thermal DAP

- Bondwires connect IC to pins
- Good thermal performance
- Higher parasitic resistance and inductance
- Larger than QFN

HotRod™ QFN

- Copper pillars (bumps/posts) on IC soldered directly to the lead-frame
- Poor thermals, compared to DAP
- Reduced parasitic resistance and inductance
- Smaller than SOIC
Thermal Path for Exposed Pad Packages

- **PowerPad™ QFP/TSSOP, QFN**
  - Typical power: 0.5-10W
  - Thermal design for these packages:
    - Soldered to PCB thermal/GND plane
    - PCB has thermal pad and vias tied to ground plane
    - Most of the Heat uses the Exposed Pad, because that is the lowest thermal impedance path
Thermal Path for HotRod™

- Flipped Die on Lead Frame (HotRod™)

- Typical power: 0.5-3W
- Thermal design for these packages:
  - Large Pads connected to Power Devices are essential to distribute heat.
    - Most of Heat is through large pads because of metal routing but pins can also distribute heat
      » PGND, GND, SW: Most effective
Thermal Layout for HotRod™

Fat and Wide Traces on $V_{\text{IN}}$, GND, SW

NOTE: Tradeoff on SW pin for EMI and Thermal

Lots of GND vias
• Values of $\theta_{JA}$ given in the table are **NOT** useful for thermal design
  – They are useful for comparing packages within TI or with our competitors

• The other values can be useful
  – $\theta_{JC}$, $\Psi_{JB}$ and $\Psi_{JT}$ are the most useful

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>SOIC</th>
<th>HotRod™</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DA}$</td>
<td>42.9</td>
<td>72.5</td>
</tr>
<tr>
<td>$R_{BJC\text{ (top) }}$</td>
<td>54</td>
<td>35.9</td>
</tr>
<tr>
<td>$R_{BJB}$</td>
<td>13.6</td>
<td>23.3</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>4.3</td>
<td>0.8</td>
</tr>
</tbody>
</table>

**THERMAL METRIC:**
- $R_{DA}$: Junction-to-ambient thermal resistance
- $R_{BJC\text{ (top) }}$: Junction-to-case (top) thermal resistance
- $R_{BJB}$: Junction-to-board thermal resistance
- $\Psi_{JT}$: Junction-to-top characterization parameter
Thermal Characteristics Table in Data Sheet

• The values given in the table are simulations
  – The traces on the JEDEC board are too small to provide adequate heat-sinking
    • For HotRod™ the heat is mostly dissipated from the pads
      – This makes the JEDEC board a bad estimate for thermals

• JEDEC uses the same standard for all packages
  – This makes the numbers good for comparing packages

• Need better methods for estimating $\theta_{JA}$
Designing a PCB for Thermal Performance
Design Strategy Summary

1. Calculate $P_D$ based on the efficiency and system inputs: $T_A$, $V_{IN}$, $V_{OUT}$, $I_{OUT}$

2. Calculate required $\theta_{JA}$

3. Determine required board size
   - Datasheet guidelines
   - SNVA419C spreadsheet
   - Online calculator
   - WebTHERM™/Webench

4. Follow Layout Guidelines for vias, and routing, etc.
Example:

Scenario:

Customer: “I have this input voltage, output voltage, output current and ambient temperature”

“Is it going to work OK thermally?”

How much board space/heat sinking do I need with this device?

• Step 1: Estimate the IC power dissipation.

• Step 2: Determine Thermal Requirements

• Step 3: Determine Board Size Based on Thermal Requirements
Step 1. Estimate the IC Power Dissipation

1a. Look in the datasheet for an efficiency curve that is close to the given application conditions. Ideally the efficiency should be taken at a temperature greater than 25°C, since the die will always be above ambient when running with load.

1b. Calculate the total power loss using:  \[ P_{\text{LOSS}} = V_{\text{OUT}} \cdot I_{\text{OUT}} \cdot \left( \frac{1-\eta}{\eta} \right) \]

1c. Subtract the loss in the inductor to get the IC \( P_{D} \):  \[ P_{D} = P_{\text{LOSS}} - I_{\text{OUT}}^{2} \cdot R_{L} \]

\[ R_{L} = \text{Inductor DCR} \]
Step 1. (cont.)

Example: LMR33630 RNX (Hot Rod)  \( V_{\text{IN}} = 12\text{V}, \ V_{\text{OUT}} = 5\text{V}, \ I_{\text{OUT}} = 3\text{A}, \ 2.1\text{MHz} \)

1a. We find an efficiency from the data sheet:

Approximate Efficiency of 91%

based on graph shown

1b. \( P_{\text{LOSS}} = 1.48\text{W} \)

1c. \( P_{\text{D}} = 1.16\text{W} \ (R_L \sim 35\text{m}\Omega \text{ from EVM user guide}) \)
Step 2. Calculate maximum allowable $\theta_{JA}$

For this step we need the maximum ambient temperature from the application requirement and the maximum junction temperature from the data sheet.

\[ T_A = 85°C \]
\[ T_{J_{\text{max}}} = 150°C \]

\[ \theta_{JA} \leq \frac{T_{J_{\text{max}}} - T_A}{P_D} \]

We get $\theta_{JA} \leq 56°C/W$

A quick start calculator is also available to help with “what-if” calculations:
Step 3. Estimate the PCB Copper Area

OPTIONS:
A. Datasheet $\theta_{JA}$ vs Copper Area Curves (Easiest Option if available)
B. Thermal Estimate Based Excel Calculator
C. PCB Thermal Calculator online or other simulation tools
D. Webench Thermal Simulation
Step 3: Option A – Data Sheet Curves

This option is more accurate since it based on measured data. The curves for **LMR33630** are shown below:

This curve indicates that a 4 layer board with an area of 4.0 cm x 5.0 cm (20 cm²) will give $\theta_{JA} < 56^\circ$C/W
Step 3: Option B – Thermal Estimator Excel

- Application Note SNVA419C and the associated spread-sheet can be used to estimate the required board size for a given set of conditions
  - Allows you to play “what-if” scenarios
  - Works well for packages with a DAP
    - Need to “adjust” values of $\theta_{JC}$ for other package types
Step 3: Option C – Online PCB Calculator

http://www.ti.com/adc/docs/midlevel.tsp?contentId=76735

Only available for some IC packages
Step 3: Option D  Webench / WebTHERM™

https://webench.ti.com/webench5/power/webench5.cgi
Step 3: Option D   Webench / WebTHERM™

Customize LMR33630AQRNXRQ1 - 12V-24V to 5.00V @ 3A

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC Tj</td>
<td>44.14 °C</td>
<td>IC junction temperature</td>
</tr>
<tr>
<td>IC Pd</td>
<td>1.13 W</td>
<td>IC power dissipation</td>
</tr>
<tr>
<td>Iin Avg</td>
<td>683.5 mA</td>
<td>Average input current</td>
</tr>
<tr>
<td>ICTthetaJA Effective</td>
<td>12.5 °C/W</td>
<td>Effective IC Junction-to-Ambient Thermal Resistance</td>
</tr>
<tr>
<td>IC Iq Pd</td>
<td>1.85 mW</td>
<td>IC Iq Pd</td>
</tr>
</tbody>
</table>

Note: All above values are estimates. For more accurate values, please run electrical simulation.
Step 3: Data Sheet De-Rate Curves

• Many data sheets will have a “de-rating” curve
  – This shows the maximum load current for a given ambient temperature
  – Taken with one particular $\theta_{JA}$
  – Uses the efficiency taken at an elevated temperature
    • 85°C or 125°C

![Graph showing maximum output current vs ambient temperature]

Figure 24. Maximum Output Current vs Ambient Temperature

$V_{IN} = 12 \text{ V}$
$V_{OUT} = 5 \text{ V}$
$f_{SW} = 400 \text{ kHz}$
$R_{LUA} = 30^\circ\text{C/W}$
Effects of Copper Area (TPS54824)

Comparing the 2 different copper area, at higher current of 8A, the improvement of case temperature ~ 20°C

Step 4: Layout Guidelines – Copper Thickness

- Use appropriate copper thickness
- 1 oz copper thickness is 35µm and 2 oz copper thickness is 70 µm
- At least 1 oz copper is recommended for all DC-DC converter designs.
- 2 oz copper is recommended for designs that dissipate more than 3 Watts

**Example:** For a copper area of 3 inches x 3 inches:

- 1 oz copper: $\theta_{JA} \approx 28^\circ\text{C/W}$
- 2 oz copper: $\theta_{JA} \approx 21^\circ\text{C/W}$
- About 25% improvement

\[
\theta_{CU} = \frac{1}{\lambda_{CU}} \cdot \text{Length} \div \text{Width} \cdot \text{Thickness}
\]
Step 4: Layout Guidelines – Vias

- Use lots of vias
  - Thermal resistances in parallel
  - The more you add, the lower the resistance is.

- Typical 0.3mm (12mil) thermal vias with 17.5μm (0.5oz) plating
- 1.56mm (62mil) PCB thickness

\[ \theta_{\text{vias}} \approx \frac{251}{\text{no. of vias}} \]

- More thermal via guidelines in Application Notes SNVA419C and AN-1520

Via Array Thermal Resistance Calculations:

Microsoft Excel Worksheet
Step 4: Layout Guidelines – Cuts in Copper Planes

- Cut copper plane parallel to heat flow

![Diagram showing different thermal patterns with temperatures 115°C, 121°C, and 117°C.](image)
Step 4: Layout Guidelines – “Pizza Slice”

1. IC is the heat source and “tiny” compared to PCB
2. Maximize so that heat is radiating in all 360 degree directions of top and bottom copper plane
3. Ideally, heat source is placed in center of a PCB
4. If the tip of the “slice” is not touching the heat source properly then the whole “slice” can not efficiently contribute as heat sink
5. Make thermal cuts only in heat flow directions
6. Maximize total copper area, number of layers and Cu thickness on PCB
7. Utilize the bottom copper side of PCB
8. Use all available external components like Inductors, resistors and ceramic caps as potential heat conductors to bridge to colder areas / slices
9. Use larger components like connectors and aluminum caps to improve heat sinking of slices
Step 4: Layout Guidelines – Optimum Cuts

Non-optimized PCB design

- Die Temp = 124°C
- $\Theta_{JA} = 32^\circ\text{C/W}$

Thermally Optimized PCB

- Die Temp = 88.3°C
- $\Theta_{JA} = 20.4^\circ\text{C/W}$

Thermal Bottlenecks

Large Copper “Slices”
Step 4: Layout Guidelines – High Current Vias

High Current Via Requirements:
- 1A/via max <14mil diameter
- 2A/via max >14 mil diameter
- 5A/via max >40 mil diameter
- Don’t block high current paths with vias
Step 4: Example of vias near the IC (TPS54824)

Figure 8. TPS54824EVM-779 Rev. A vs Rev. B. Top Layer Layout


Measured Case Temperature vs Load Current With Different EVM Revisions

\[ V_{IN} = 12 \text{ V} \]

\[ T_A = 23 \degree \text{C} \]

\[ V_{OUT} = 1.8 \text{ V} \]

10-minute soak time
Step 4: Via Density near the IC

Other Considerations – Thermal Coupling & Footprint

• Thermal Coupling
  – Devices in a system are always thermally coupled
  – Most significant when packages get closer than 2x the package dimension to each other

• Thermal Footprint
  – A thermal footprint is the area of the PCB that participates strongly in the convection and radiation from the package
  – This area is about 18x the package area as shown
    • Top of PCB and bottom of PCB count

• When thermal footprints overlap, changes in junction temperatures are dramatic
Other Considerations – Thermal Coupling Example

Separation = 50mm
Max T = 81.6° C

Separation = 25mm
Max T = 84.4° C

Separation = 8mm
Max T = 98.4° C

Separation = 12.5mm
Max T = 92.9° C
Which Thermal Performance is BETTER?

- Inductor 74438335150 (3mm x 3mm x 1.5mm)
  - 15µH, 720mΩ
- Inductor XAL4040-153 (4mm x 4mm x 4mm)
  - 15µH, 84mΩ
TEMPERATURE COMPARISON

• Operating Conditions
  – LMR36015
  – VIN = 24V
  – VOUT = 5V
  – IOUT = 1.2A
  – Switching frequency = 2.1MHz

• IC Package Temperature
  ~ 92°C

 Δ = 21°C

• IC Package Temperature
  ~ 71°C
Some Layout Best Practices

• Spread out hot devices on PCB

• Maximize GND layer in PCB

• No breaks in heat flow through planes

• Increase PCB layers or thickness

• Widen PCB traces near device

• Thermal vias under or near device

• Airflow (global and local)
Quiz......layout review

LM53625
2.5A Synchronous Buck Converter 2.1MHz
Example Design Calculation
LMR33630 SOIC and LMR33630 Hot Rod
LMR33630 Case Study

Scenario:

I have a design with the following specifications:

VIN = 6V to 18V with a typical value of 12V

VOUT = 3.3V

IOUT = 3A

Operating Frequency = 2.1MHz

How does the Hot Rod package compared with SOIC?
Can the Hot Rod Package handle my thermal requirement?

Should I stick with SOIC with DAP Package?

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)(2)</th>
<th>LMR336x0</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DDA (HSOIC)</td>
<td>RNX (VQFN)</td>
</tr>
<tr>
<td><strong>8 PINS</strong></td>
<td><strong>12 PINS</strong></td>
<td></td>
</tr>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>42.9(2)</td>
<td>72.5(2)</td>
</tr>
<tr>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>54</td>
<td>35.9</td>
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<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
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<td>13.8</td>
<td>23.5</td>
</tr>
<tr>
<td>(R_{JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>4.3</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) The value of \(R_{JA}\) given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see Maximum Ambient Temperature section.
LMR33630 Efficiency Comparison

At 12V input and 3A
Efficiency ~ 84%

At 12V input and 3A
Efficiency ~ 88%
LMR33630 Power Dissipation Comparison

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SOIC</th>
<th>HOT ROD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>84%</td>
<td>88%</td>
</tr>
<tr>
<td>Total Power Loss ( P_{LOSS} )</td>
<td>1.88 W</td>
<td>1.35 W</td>
</tr>
<tr>
<td>Inductor DCR (( R_L )) (from EVM)</td>
<td>25 mΩ</td>
<td>35 mΩ</td>
</tr>
<tr>
<td>Power Dissipated DCR</td>
<td>0.225 W</td>
<td>0.315 W</td>
</tr>
<tr>
<td>Power Dissipated IC (( P_D ))</td>
<td>1.655 W</td>
<td>1.035 W</td>
</tr>
</tbody>
</table>

The Hot-Rod Package dissipate less power compared to SOIC part
LMR33630 EVM Board Size Comparison

**SOIC**

Board area = 3.2 inch x 2.6 inch = 8.32 inch$^2$ = **53.6 cm$^2$**

**HOTROD**

Board area = 3.0 inch x 2.8 inch = 8.4 inch$^2$ = **54.2 cm$^2$**
LMR33630 $\theta_{JA}$ Comparison

**SOIC**

- $\theta_{JA} \approx 25 \degree C/W$

**HOTROD**

- $\theta_{JA} \approx 47 \degree C/W$

Board area = **53.6 cm$^2$**

Board area = **54.2 cm$^2$**
### LMR33630 Expected Temperature

**PARAMETER** | **SOIC** | **HOT ROD**
--- | --- | ---
Power Dissipated IC ($P_D$) | 1.655W | 1.03 W
Junction to Ambient Thermal Resistance ($R_{θJA}$) | ~ 25 °C/W | ~ 47 °C/W
Temperature Rise | $1.655 \text{ W} \times 25 \degree \text{C/W} = 41.3\degree \text{C}$ | $1.03 \text{ W} \times 47 \degree \text{C/W} = 48.4\degree \text{C}$
At 25°C Ambient | ~ 66 °C | ~ 73 °C
Measured Case Temperature = 61°C
With $\Psi_{JT} = 4.3^\circ$C/W
Junction Temperature ~ 68°C

Measured Case Temperature = 67°C
With $\Psi_{JT} = 0.8^\circ$C/W
Junction Temperature ~ 68°C
Example Summary

1) $R_{\theta JA}$ value given in the datasheet thermal table should not be used to measure thermal performance of the IC

2) The value is only useful to compare packages within TI and our competitors

3) $R_{\theta JA}$ curves within the datasheet can be used to predict the temperature of the IC for a given copper size area

4) Some datasheet will also show derating curves for a specific $R_{\theta JA}$ value
Thank you