Top 10 gate driver pitfalls and how to address them
By John Geiger

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What will I get out of this session?

Purpose:

- Gate Driver Fundamentals
- Common issues, solutions and design practices on
  1. Bias supply
  2. Open functional pins or connect with Hi-Z
  3. Parasitics
  4. dv/dt noise
  5. Variance

- Part numbers mentioned:
  - UCC27712-Q1
  - UCC27211A-Q1
  - UCC21222-Q1
  - UCC21520-Q1

- Relevant applications:
  - On Board Charger
  - DC/DC Converter
  - Motor Drive
Where are gate driver ICs used?

- Electric vehicles
- Class D audio
- Renewables
- Solid state lighting (SSL)
- Adaptors and chargers
- Server/telecom/UPS
- Li-ion battery portables
- Motor drive (VFD)
- Portables
- Gate driver applications
What are the power devices?

<table>
<thead>
<tr>
<th></th>
<th>Si-MOSFET</th>
<th>IGBT</th>
<th>SiC-MOSFET</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage ratings</td>
<td>20~650V</td>
<td>≥650V</td>
<td>≥650V</td>
<td>≤650V</td>
</tr>
<tr>
<td>Optimal $V_{GS}$</td>
<td>0~15V (±20V)</td>
<td>-10~15V (±20V)</td>
<td>-5<del>20V (-10</del>25V)</td>
<td>-5<del>10V (±18V) (-10</del>7V)</td>
</tr>
</tbody>
</table>

- **Si-MOSFET**: 10V
- **IGBT**: 12V
- **SiC-MOSFET**: 20V 18V 16V
- **GaN**: 5V 4V 3V 2V

-I-V curves are from datasheets of Infineon, Fairchild, ST, CREE, EPC.
Turn-ON/OFF process

Switching on loss

\[ \int_{t_1}^{t_3} V_{DS}(t) \cdot I_D(t) \, dt + E_{OSS} \]

\[ t_{1 \sim 3} \propto \frac{1}{I_{Drv}} \]

Stronger driver \( \rightarrow \) lower switching loss
#1 What is wrong with VCC?

**Causes**
- Low capacitance on VCC
- Capacitor placement/layout
- Biased capacitance (C vs. V)
- Temperature (Capacitance vs. Temp)
- Capacitance aging

**Consequences**
- × Driver malfunction
- × UVLO tripping
- × EMI noise
“It was working yesterday!”

Day 1: Switching “normally” and left to run overnight

Day 2: Constantly missing high side pulses… UVLO is being triggered…

Something shifted overnight...

After 24 hrs, the capacitance of an X5R dielectric cap will drop by ~15%

Design Guidelines: Consider duty cycle limitations of bootstrap supply after derating for voltage, temperature, and aging
What is wrong with HO waveform?

• Causes
  – Low capacitance
  – Low Rgs
  – Low Fsw
  – Large D, on HO

• Consequences
  ❌ Hot MOSFET
  ❌ Output ripple
  ❌ HO drooping

Sizing Bootstrap Capacitor

• \( C_{\text{Boot}} = \frac{Q_{\text{Total}}}{\Delta V_{HB}} \)
• \( Q_{\text{Total}} = Q_G + (I_{\text{HBS}} \times D_{\text{Max}}/F_{\text{SW}}) + (I_{\text{HB}}/F_{\text{sw}}) \)
#2 What is wrong with switch node waveform?

Design Guidelines
- Reduce $R_{\text{Boot}}$
- Minimum bottom switch ON time

- HS waveform – Inconsistent HS signal
- Very short LO duty cycle – Partially charged $C_{\text{Boot}}$
What do you think of this layout?

- Bypass capacitor need to be as close to gate driver IC as possible
- VCC, VDD, input filter, DT, EN, DIS
- Value and package of the capacitor do matter
#3 Is this waveform normal?

- HS Neg. ringing → overcharging the boot cap
- Fast HS slew rate → noise and oscillation on HB

Design Guidelines
- Increase boot resistor
- Increase boot capacitor
- Minimize board parasitics
Boot voltage overcharge with eGaN

- Negative turn-off bias, -4V, increases the reverse Source-Drain voltage
- High side bootstrap supply over charges
- Driver VDD > $V_{GS\text{Max}}$ → eGaN Gate Breakdown

ISO power supply for gate driver Bias
#4 Why is there NO gate driver output?

- VDD supply is ready
- Driver IC is enabled
- PWM input HI&LI is ready
- The low side LO is good.
- High side boot supply is charged when LO starts switching
#4 Why is there NO gate driver output?

- VDD supply is ready
- Driver IC is enabled
- PWM input HI&LI is ready
- The low side LO is good.
- High side boot supply charged when LO starts switching

- There is NO high side output

- **UVLO Delay**: 5us to 100us depends on the driver
#4 Why is there NO gate driver output?

Design Guidelines
- Turn-on low side to pre-charge boot capacitor
- Synchronize HI and LI

Synchronization LI and HI after Bias supplies are both ready.
#5 What is wrong with the waveform? Remedies?

Design guidelines:

- Input filter to improve overall system performance
- Decrease loop inductance in PCB layout
#6 What causes glitches in PSFB at full load?

- Voltage waveform “VAB” has intermittent failure and glitches
What causes glitches in PSFB at full load?

Output A is being delayed by 1.2us (which should be <50ns)
#6 What causes glitches in PSFB at full load?

- Do NOT leave functional pins open

Design Guidelines:
- DT pin is left open, and noise is coupled into the driver
- For dead time setting, bypass with $\geq 2.2\text{nF}$ close to DT pin
  \[ \text{DT (in ns)} = 10 \times \text{RDT (in kΩ)} \]
- For overlapping or no DT, tie DT pin to VCCI
Parasitics in gate driver subsystem

\[ C_{\text{ISS}} = C_{GS} + C_{GD} \]
\[ C_{\text{RSS}} = C_{GD} \]
\[ C_{\text{OSS}} = C_{GD} + C_{DS} \]
#7 What is wrong when HO turns off?

- High voltage and IGBT applications
- Series gate and gate to source resistor
- Driver with Miller clamp

- High dV/dt and dl/dt causes D-G capacitor to charge and develop voltage
- Voltage may be higher than Vgs(th)
#8 Why is the gate drive waveform oscillating?

- Increase turn-on loss
- Higher di/dt, EMI
- Device overshoot
- Gate drive oscillation (over/under shoot)
#8 Why is the gate drive waveform oscillating?

- Slow down body diode reverse recovery
- FET with robust and low $Q_{RR}$ body diode
- Soft switching - ZVS

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Parasitics

V$_{GS}$ 15V/div
I$_{ds}$ 20A/div
V$_{DS}$ 100V/div
80ns/div

H-Bridge Gate Driver
Parasitic Diode

Driver IC

SW

Ferrite Bead

Texas Instruments
Minimize high current gate drive loops

- Gate driver outputs carry high currents and therefore minimize the output loop
- If totem pole buffer is used, then place it as close to the power MOSFET as possible
- Gate driver output ground and power MOSFET source need to be as short as possible

Gate drive and power train layout key to reducing overshoot, ringing and EMI!
#9 What is wrong with my output?

- Case 1: Output is Shorter than Input
  
  **❌ HO 80ns Glitches at HI=High**
  - Double pulse on HI
  - LI pulled down w/ 4.7kΩ
#9 What is wrong with my output?

- Case 2: Output is Longer than Input
  
  - **HO Stretched for 4\(\text{us}\) more**
    - Double pulse on HI
    - LI pulled down with 4.7kΩ
#9 What is wrong with my output?

- Case 3: Output on and off intermittent while HI is ON

  - **HO turns off intermittent**
    - Double pulse on HI
    - LI pulled down w/ 4.7kΩ
The switch node CMTI is >200V/ns

- Slow down BD reverse recovery
- FET w/ low $Q_{RR}$ B-diode
- Soft switching - ZVS

Very high switch node $dV/dt$ results in EMI challenges
Layout – Ground Plane And Switch Node (SW)

Gate drive and power train layout key to reducing overshoot, ringing and EMI!

- Minimize or avoid overlapping switch node plane and ground plane
- Could create issues when switching frequencies are high
- As HS slew rates are high, overlap of ground plane and switch node plane might inject noise in other circuits on the board
Would This Waveform Create Any System Problem?

- HO/LO might cross conduct
- Shoot-through current
- Excessive power dissipation
- False overcurrent tripping

- Account for propagation delay and delay matching variation across temperature/voltage
- Account for drive strength variation across temperature/bias voltage
Summary

- Various issues encountered while designing switch-mode power supplies were discussed from the gate driver IC point of view and their resolutions were clearly identified.
- Proper bypassing of the gate driver IC (as with many other ICs) is extremely critical to its performance.
- When gate driver IC is used in half-bridge configuration, switch node slew rate plays an important role in the performance of the gate driver IC.
- PCB layout plays important role in satisfactory performance of the gate driver IC and thus the whole system.
Non-isolated half-bridge gate drivers are used in vast applications and end-equipments like DC-DC converters, motor drives, belt starter-generator, and electric power steering.

Customers are looking for higher power density, higher efficiency, and more robustness but they are extremely price sensitive.

**TI’s answer.... UCC27282** 120V half-bridge driver:
- 5V UVLO
- 3.5A drive current
- Interlock/cross-conduction protection
- Enable/disable pin
- Best negative voltage handling
- 3mm x 3mm SON package

**Customer Care-abouts**

- **DENSITY** Small package enables use in applications where board space is a premium.
- **EFFICIENCY** Low UVLO, better drive strength, and better switching characteristics enables higher switching frequencies while keeping switching losses low and thereby improved efficiency.
- **ROBUSTNESS** Interlock, enable/disable functionality, and negative voltage handling capability enables use in harsh environments.

**Method**

- Recorded bench data from competitor parts and TI’s UCC27282 to show Golden Gate’s better performance over competition. Synchronous-Buck tested at 48 VIN, 200kHz, 96W.
- UCC27282 can provide more current at lower V_DD levels than competition for better efficiency.
- UCC27282 has shorter rise and falls times especially at lower V_DD levels.
- UCC27282 is more efficient especially at low V_DD.

**Results**

**Competitor’s Limitations**

- UCC27282 is specified to handle negative 5V at its inputs while competition is not.
- UCC27282 is specified to handle negative 2V at its outputs and negative 14V on HS. Competition is not.

**Call to Action**

- Upgrade your current 100 half-bridge drivers to the all-new UCC27282 gate driver, which will deliver higher performance and more robustness.

**Evaluation Samples Available**

**Industrial Version**