Input Offset Voltage ($V_{OS}$) & Input Bias Current ($I_B$)

Multiple Choice Quiz

TI Precision Labs – Op Amps
Quiz: Input Offset Voltage ($V_{OS}$) & Input Bias Current ($I_B$)

1. Which amplifier would have the highest bias current?
   a. CMOS
   b. Bipolar
   c. Bipolar with input bias cancellation.
   d. High speed.

2. Which amplifier would have the lowest offset voltage?
   a. Zero drift amplifier
   b. High speed CMOS
   c. High speed bipolar

3. Texas Instruments SPICE models target the _______ specifications.
   a. Maximum
   b. Typical
   c. High grade
   d. Low grade
Quiz: Input Offset Voltage ($V_{OS}$) & Input Bias Current ($I_B$)

4. A typical offset of 10uV indicates _______.
   a. The average offset is 10uV
   b. 100% of the devices will have an offset less than 10uV
   c. 50% of the devices will have an offset less than 10uV
   d. standard deviation is equal to +/-10uV

5. A maximum offset of 100uV indicates _____.
   a. 90% of the devices are less than 100uV.
   b. The device was tested with 100uV limits and only passing units were c. shipped.
   c. Applying more than 100uV will damage the unit.
   d. Offset can range from 0 to 100uV

6. Bias current is modeled as __________
   a. A current source in series with each input.
   b. A current source connected to each input with respect to ground.
   c. A resistance between the amplifier inputs.
Quiz: Input Offset Voltage ($V_{OS}$) & Input Bias Current ($I_B$)

7. Which are examples of an op amp test condition?
   a. The maximum allowable input signal, and maximum supply.
   b. The input common mode voltage, output load, and power supply voltage.
   c. The input bias current, input offset current, and offset voltage.
   d. Amplifier gain bandwidth and slew rate.

8. What is a factor that can affect bias current?
   a. Supply voltage
   b. Input signal voltage.
   c. Temperature
   d. Input offset voltage

9. Which is the primary cause of bias current in a CMOS amplifier?
   a. ESD diode leakage.
   b. Gate leakage
   c. Parasitic capacitance
   d. Semiconductor defects
Quiz: Input Offset Voltage ($V_{OS}$) & Input Bias Current ($I_B$)

10. Offset voltage can range from ____.
   a. fV to nV  
   b. pV to uV  
   c. uV to mV  
   d. mV to V

11. Bias current can range from ___.
   a. fA to nA  
   b. pA to mA  
   c. uA to A

12. Bias current cancellation is a technique ___.
   a. Used in CMOS amplifiers to cancel Ibos.  
   b. Used in Bipolar amplifiers to minimize bias current.  
   c. An external circuit used to cancel op amp bias current.
Quiz: Input Offset Voltage ($V_{OS}$) & Input Bias Current ($I_B$)

13. What type of circuit would have the largest error from bias current.
   a. A bipolar amplifier with a small source resistance.
   b. A bipolar amplifier with a large source resistance.
   c. A CMOS amplifier with a small source resistance.
   d. A CMOS amplifier with a large source resistance.

14. Input offset voltage drift is _______.
   a. A change in offset voltage over temperature
   b. A change in offset voltage over time.
   c. A change in offset voltage with different common mode voltages
   d. A change in offset voltage with different power supply voltages.

15. If a maximum specification is not given you can estimate the maximum by ____.
   a. Multiplying the input by 10.
   b. Doubling the typical
   c. Looking at the distribution.
   d. Comparison to similar devices.
Input Offset Voltage ($V_{OS}$) & Input Bias Current ($I_B$)

Multiple Choice Quiz: Solutions

TI Precision Labs – Op Amps
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