Low Distortion Design – 2
TIPL 1322
TI Precision Labs – Op Amps

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Prerequisites: Noise 1 – 3
(TIPL1311 – TIPL1313)
A Simplified Internal Op Amp Design
A Basic Op Amp Input Stage

A basic op amp input consists of:
- A differential pair (Q1, Q2)
- A current mirror active load (Q3, Q4)
- A tail current source (IT)

\[ I_O \approx I_T \cdot V_{\text{DIFF}} / 2 \cdot 26\text{mV} \]
Input Stage Transfer Function

- Ideal output current:

\[ I_O \approx I_T \cdot \frac{V_{DIFF}}{2 \cdot V_T} \]

- Real output current:

\[ I_O = I_T \cdot \tanh \left( \frac{V_{DIFF}}{2 \cdot V_T} \right) \]
Input Stage Transfer Function

• Tailor series of the hyperbolic tangent function (tanh):

\[ I_O = \frac{I_T}{2V_T} V_{DIFF} - \frac{I_T}{24V_T^3} V_{DIFF}^3 + \frac{I_T}{240V_T^5} V_{DIFF}^5 \ldots \]

• Note: Distortion depends on input differential voltage (\(V_{DIFF}\))
• More op amp open loop gain (\(A_{OL}\)) means less input stage distortion

\[ V_{DIFF} = \frac{V_O}{A_{OL}} = \frac{V_{IN}}{1 + A_{OL} \beta} \]
Recognizing Input Stage Distortion

• Elevated 3\textsuperscript{rd} harmonic indicates distortion from input stage
  – 5\textsuperscript{th} harmonic will also be present

• FFT:
  – OPA227, Gain: +1
  – Load: 100k\Omega
  – 5V_{RMS}, 20kHz
  – 3\textsuperscript{rd}: -96dBc
  – 5\textsuperscript{th}: -135dBc

\[ I_O = \frac{I_T}{2V_T} V_{DIFF} - \frac{I_T}{24V_T^3} V_{DIFF}^3 + \frac{I_T}{240V_T^5} V_{DIFF}^5 \ldots \]
Slew-Induced Distortion?

- **Myth**: Below the slew rate limit, the op amp is distortion free.
- **Reality**: Distortion occurs below slew limit:

\[ SR = \frac{i_T}{C_C} \]

- **Example**: \( i_T = 100\mu A, C_C = 20\text{pF} \)

\[ SR = \frac{100\mu A}{20\text{pF}} = 5V / \mu s \]
Slew-Induced Distortion?

- Slew rate limitation:

\[
\frac{SR}{2\pi f} = \frac{2.3 \text{ V/\mu s}}{2\pi(50\text{kHz})} = 7.32\text{Vpk} = 5.18\text{Vrms}
\]

- Input stage distortion always appears before slew rate distortion

- Slew rate limitation does increase distortion at high output levels

**Graph:**

- THD+N vs. Output Voltage
- OPA227
- f = 50kHz
- Meas. BW = 250kHz

- Input Stage Distortion
- Slew-Induced Distortion
Input Crossover Distortion

• Rail-to-rail inputs 2 differential pairs
  – PMOS for common mode input voltages: \( V_{EE} \) to \( V_{CC}-1.8V \)
  – NMOS for common mode input voltages: \( V_{CC}-1.8V \) and above

• “Crossover region” where both inputs are conducting
  – DC offset change
  – Shift in AC parameters

• The offset of the NMOS pair may be untrimmed
  – Causes a sudden change in input offset voltage of the op amp
Input Crossover Distortion

• Non-Inverting Amplifiers
  – Input signal passes through crossover region
    • Additional offset is summed with the input signal
  – Additional offset distorts the signal
  – Typically high-order harmonics

![Graph of V_{CM} vs. V_{OS} with OPA172 labeled]
Example of Input Crossover Distortion

OPA2172: Gain +1, 5V\(_{\text{RMS}}\)\(7.07V_{\text{pk}}\)/1kHz signal, 100kHz load

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
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<tr>
<td>(V_{\text{CM}})</td>
<td>Common-mode voltage range(^{(1)})</td>
<td>((V-) - 0.1\ V)</td>
<td>((V+) - 2\ V)</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

No Crossover Distortion

Crossover Distortion

+/-10V Supplies

+/-9V Supplies

\(^{(1)}\) Common-mode voltage range

Texas Instruments
Common-Mode Input Impedance Variation

- Meas. Bandwidth = 500kHz
- THD+N Comparison at 10kHz
  - Rs = 0, -104dB
  - Rs = 10kΩ, -73dB
CM Impedance Variation

- Common-mode input impedance varies with $V_{cm}$
  - This distorts the input voltage waveform
  - Worst in non-inverting, low gain, high source impedance

- Input capacitance variation
  - JFET Input Op Amps:
    - Gate-to-substrate capacitance
    - ESD Diodes
  - BJT Input Op Amps:
    - Collector-base junction capacitance
    - ESD Diodes
  - CMOS Input Op Amps
    - ESD Diodes

- Input resistance variation
  - Mismatch in leakage of ESD diodes
  - Beta of input transistors varies with $V_{CE}$ and $I_C$
Improving Performance: Match Impedance at Inputs

- Adds additional noise
- May cause stability problems!

THD+N vs. Frequency

- Rs = 10kΩ, Rf = 0Ω
- Rs = 10kΩ, Rf = 10kΩ
- Rs = 0Ω, Rf = 0Ω

Diagram of OPA1602 circuit with 5Vrms input and 10kΩ, 100kΩ resistors.
Improving Performance

• Best Performance: dielectrically isolated JFET-Input
  – Absolute best:
  – OPA827, OPAx140/x141/164x
  – Very good: “DiFET” op amps: OPA2107, OPA627, etc.

More information:
“Distortion and Source Impedance in JFET Input Op Amps” –Caldwell, 4Q2014AAJ
Rules for Minimizing Input Stage Distortion

• Minimize Op Amp Input Differential Voltage ($V_{DIFF}$)
  – Reduce output voltage (not usually an option)
  – Reduce gain (may not be an option)
  – Maximize $A_{OL}$
    • High supply voltages
    • Select parts with proper GBW

• Prevent Input Crossover Distortion
  – Observe input CM voltage range in datasheet
  – Use inverting amplifier topology
  – Use zero-crossover distortion op amps: OPA320, OPA322, OPA365

• Prevent Common-Mode Impedance Effects
  – Use inverting amplifier topology
  – For non-inverting amplifiers match impedances at both op amp inputs
  – Select parts with dielectrically isolated JFET inputs:
    • OPAx140/x141/164x, OPA827, BB DiFET OPAs (OPA627, OPA2107, etc)
Thanks for your time!
Please try the quiz.