Inside the Delta-Sigma Converter: Practical Theory and Application

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ADC Technologies

Converter Resolution (bits) vs. Conversion Rate (SPS)

- **Delta Sigma**
- **SAR**
- **Pipeline**

Conversion Rate (SPS):
- 10
- 100
- 1K
- 10K
- 100K
- 1M
- 10M
- 100M
- 1G

Converter Resolution (bits):
- 8
- 12
- 16
- 20
- 24
- 32

Approximate converter performance:
- Delta Sigma: High resolution at lower conversion rates
- SAR: Medium resolution with a range of conversion rates
- Pipeline: High conversion rates at lower resolution
Oversampling
Looking at the FFT of a sine wave at the output of the ADC

We see:

• Single tone

• Lots of random noise extending from DC to Fs/2 (quantization noise)

\[ \text{SNR} = 6.02 \cdot N + 1.76 \text{dB for an N-Bit ADC} \]
Oversampling $k$ times

Average noise floor has dropped – but…

SNR stays the same as before

Noise energy has just been spread over a wider frequency range
What can you gain by oversampling?

Oversampling by factor 4x increases SNR by 6dB
= Gain of 1 Bit in resolution

Oversampling alone is not sufficient to achieve a resolution of 24Bit
Inside Delta-Sigma Converter

Basics
Nuts and Bolts of Delta-Sigma A/D Converters

SAMPLE RATE (Fs)

DATA RATE (Fd)

Fs / Fd = DR
(DR = Decimation Ratio)
Modulator Output

Analog Input → Delta-Sigma Modulator → Digital Filter → Decimator → Digital Decimating Filter

Digital Decimating Filter (usually implemented as a single unit) → Digital Output
Believe it or not, the sine wave is in there!
(drawing is approximate)
1st order Delta-Sigma Modulator

Signal input, $X_1$

Difference Amp

Integrator

Comparator (1-bit ADC)

1-bit DAC

To Digital Filter

Latch

Modulation Clock

$X_1$ $V_{max}$ 0V
$X_2$ $+V_{max}$ $-V_{max}$
$X_3$ $+V_{max}$ $-V_{max}$
$X_4$ 1 0
$X_5$ $V_{max}$ 0V
Modulator Output Signal

TIME DOMAIN

FREQUENCY DOMAIN

Believe it or not, the sine wave is in there!

(drawing is approximate)
Multi-Order Delta-Sigma Modulators

- 1st Order ΔΣ Modulator
- 2nd Order ΔΣ Modulator
- 3rd Order ΔΣ Modulator

Frequency vs. $F_S$
Digital Filter & Decimation

Analog Input \(\leadsto\) Delta-Sigma Modulator \(\rightarrow\) Digital Filter \(\rightarrow\) Decimator \(\rightarrow\) Digital Output

SAMPLE RATE (\(F_s\))

DATA RATE (\(F_d\))

\(F_s / F_d = DR\) (DR = Decimation Ratio)

Digital Decimating Filter
(usually implemented as a single unit)
Averaging Filters

DC input levels

0V

Full-scale

Delta-Sigma Modulator

1-bit data

1-bit data streams

1/2 full scale input

1/4 full scale input

3/4 full scale input

1

0

1

0

1

0

1

0

1

0

1

0

1

0

Average

= 0.5

Average

= 0.25

Average

= 0.75

1

0

1

0

1

0

0

0

0
Filtering the Shaped Noise

Modulator provides ≥9dB improvement in SNR for every doubling of sampling rate
Decimator Function: Pick & Dump

Output Signal after Digital Filter

Output Signal after Decimator

@ Sampling Rate

@ Data Rate
Decimation Ratio

\[ \frac{F_s}{F_{\text{data}}} = \text{OSR} = \text{DR} = K \]

- \( F_s \): Modulator Frequency
- \( F_{\text{data}} \): Output Data Rate
- \( \text{OSR} \): Over Sampling Ratio
- \( \text{DR} \): Decimation Ratio

Slower output data rate / higher oversampling ratio gives better resolution.
Digital Filter Types
Filter type vs AC Performance

- 50kHz bandwidth
- Large droop
- Rising stopband
- 100dB stopband attenuation

Other 24-bit industrial ADCs

DC Response

Input Frequency (kHz)

Gain (dB)

DC
SINC vs. FIR
both have Finite Impulse Response

SINC Filter often uses CIC structure
SINC$^N$: Filter Order $N = 1$ to 5
Delay = $N \times f_{\text{data}}$
Poor attenuation above Nyquist
Zeros at $f_{\text{data}}$ can be used for 50/60Hz rejection

Forward structure
Long Filter Length e.g. $N=64$ or 128 taps
Delay = $N \times f_{\text{data}}$
Good attenuation above Nyquist
SINC Filter

- Easy economical on silicon area – low cost, low power
  - Cascaded Integrator-Comb (CIC) structure
  - No multiplication
  - No filter coefficients

- Deep notches at multiples of output data rate
  - Can be used to reject unwanted frequencies typically the line frequency
  - 50 or 60 Hz output data rate will reject 50 or 60Hz
  - 10Hz output data rate will reject both 50 and 60Hz

- Settling time (or latency) is actually very low
  Filter needs N (Order of Filter) cycles to settle
SINC Filter - Disadvantages

- Sampling theory says that we can have an input frequency up to \( \frac{1}{2} \) of the output date rate.
- However, the SINC filter response isn’t flat:
  - SINC\(^3\) filter (very common response) has \( \sim 10\)dB attenuation at this point.
  - SINC filter isn’t first choice for applications that require flat AC response, i.e digitize signals over a wide bandwidth.
- Stop band isn’t flat and attenuation at certain points may not be that high.

Note the attenuation here! Only 40dB of stop band attenuation!
Filter Order
Changing the SINC filter characteristics

• Many Delta-Sigma ADCs let the user change:
  – Decimation Ratio and/or
  – Filter Order
• This allows tradeoffs between settling time, data rate and resolution

Using a higher order filter gives better resolution
Result is longer settling time/delay
How does settling time affect throughput rate?

- Assume we have an ADC with:
  - 1kHz output date rate
  - Sinc$^3$ filter
  - 8 input channels
  - sequentially scanning the channels, one conversion on each channel

- Since we have to wait for the 4$^{th}$ conversion for a valid result, the data rate for valid output date is $1kHz/4 = 250Hz$

- Conversion rate on each channel is therefore $250Hz/8 = 31Hz$
  A long way from the 1kHz we started with

- A good reason to require a fast ADC even though the signal bandwidth is low
The FIR filter

• The FIR filter is much more like an ideal ‘brick wall’ filter
  • Nearly flat pass band followed by a rapid transition to a high attenuation stop band
• The parts that use these filters can be very fast
  • The ADS1610 is a 10MHz output date rate part (faster than our SAR converters)
• The price to pay for this is settling time / latency / conversation cycles
  • Not suitable in applications that use a multiplexer
  • Multiple channels normally use an ADC per channel (ADS1274/1278) or a SAR ADC
FIR Filter in ADS1271

- Output settling behavior after a step change on the analog input normalized to conversion periods
- X axis is given in units of conversion
- After the step change on the input occurs, the output data changes very little prior to 30 conversion periods
- The output data is fully settled after 76 conversion periods
Aliasing
The myth is that only frequencies in the area A, twice the signal bandwidth and centered on the modulator frequency can alias back to the input.

Based on this myth, the belief is that only a simple, single pole RC filter is required at the input to a delta sigma ADC because the only frequencies that can alias are well removed from the input frequency.

Customers sometimes choose a delta sigma ADC because of this very reason.

Fb- the input signal bandwidth, up to 0.5 Fdata
Delta sigma ADC’s and aliasing - exploding the myth!

What happened is that all of the frequencies in the range shown were aliased around Fdata, back to the input signal bandwidth. Fdata is as much a sampling process as is Fmod.

All of these frequencies are attenuated however by the digital filter.

Fb- the input signal bandwidth, up to 0.5 Fdata
Delta sigma ADC’s and aliasing - the truth!

All of these aliased, attenuated by the digital filter, back into the band from DC to Fb

Fdata – the output data rate
Fmod - Fb Fmod Fmod + Fb

Fb- the input signal bandwidth, up to 0.5 Fdata

• The myth assumes that the digital filter is a brick wall with a large attenuation.
  • Real filters however, as we have seen often use sinc filters and at the peaks the attenuation may only be 20-40 dB.
• This may impose a filter requirement in front of even a delta sigma ADC
Aliasing + digital Filter in Delta Sigma

Delta Sigmas with FIR filters can be used nearly up to Nyquist without Aliasing.

FIR filters good for DC and AC signals but larger Group Delay.

Delta Sigmas with SINC filters can still have Aliasing. Care must be taken with the usable range or additional AAF might be required.

SINC Filter good for DC like signals.
Application
Common Sensors
Highly Integrated

• ADS1220 Block Diagram
Ratiometric Measurement….Not!

![Graph showing Vref and Ain over time.](image)
Why Make a Ratiometric Measurement?

- \( V_{\text{ref}} \)
- \( A_{\text{in}} \)

**Time**
Why Make a Ratiometric Measurement?

- ADC Result Code \( = \left( \frac{A_{in}}{V_{ref}} \right) \times (2^n - 1) \)
- Current excitation
  - ADC Result Code
    \[ \left( \frac{i_{\text{EXCITE}} \cdot R_{\text{SENSE}}}{i_{\text{EXCITE}} \cdot R_{\text{REF}}} \right) \times (2^n - 1) = \frac{R_{\text{SENSE}}}{R_{\text{REF}}} \times (2^n - 1) \]
PGA Bypass

- ADS1220 Block Diagram
Input Common Mode

Diagram with two gains A1 and A2, connected to an ADC, with resistors R and a capacitor C.
Input Common Mode

AVDD = 3.3 V
PGA = 1

$V_{CM} \text{ Range (V)}$

$V_{IN} \text{ (V)}$

3.3 V / 4
ADS1220 Power Saving Modes

• Power Down Single Conversion
• Duty Cycle
ADS1220 Filter Response 20sps

- FIR Filter Response with 50/60Hz Rejection

![Filter Response Graph](image-url)
Thermocouple Measurement
3-Wired RTD Measurement
2-Wire RTD Measurement
Bridge Measurement

[Diagram showing a circuit with labeled components such as REFP1, REFP0, REFN0, AVDD, REFN1, AVSS, Mux, PGA, ΔΣ ADC, Digital Filter and SPI Interface, Low Drift Oscillator, Precision Temp Sensor, and connections to 5.0 V and 3.3 V power sources with 0.1 μF capacitors.]
Thank you all!!

Q & A
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