Digital Front End (DFE) Training

DFE Overview
Agenda

- High-speed Data Converter Systems Overview
- DFE High-level Overview
- DFE Functional Block Diagrams
- DFE Features
- DFE System Use Cases
- DFE Configuration
High-speed Data Converter System Overview (1)

- Signals can be represented in the time domain or frequency domain.
- In order to describe the signal processing in a high-speed data converter system on the following slides, it will be helpful to look at the signal in the frequency domain at several key places.

![Time Domain and Frequency Domain](image)

Time Domain: $P(t)$

Frequency Domain: $P(v)$
High-speed Data Converter System Overview (2)

- Processors handle data channels of interest at symbol rate.
- Digital up/down conversion and combination up-samples and moves the individual channels up or down in frequency and combines them into a higher bandwidth stream.
- The combined stream is sent across the JESD interface.
- Analog/RF processing moves the combined signal to RF so each channel ends up at the desired carrier frequency.

![Diagram showing signal flow and processing steps]

**Transmitted/Received signal at wireless/wired medium**

**Frequency**

**JESD Interface**

**Stream at JESD interface** (i.e. 60 – 368 MHz) (Zero-IF System)

**Digital processing**

**Analog processing**
High-speed Data Converter System Overview (3)

- Low-IF systems add one stage.
- The combined stream is up-converted to an Intermediate Frequency (IF) before going to RF.

![Diagram showing the process of up-conversion and channel combination for Low-IF systems.](image)
DFE High-level Overview

4x JESD204B TX
  - TX Lane 0
  - TX Lane 1
  - TX Lane 3
  - JESD204B Sync

JESD204B SYSREF (Ext.)
  - JESD204B Sync

4x JESD204B RX
  - RX Lane 1
  - RX Lane 2
  - RX Lane 3
Transmit Path
Receive Path

Color Legend
- Red: Channel Processing RX
- Purple: Stream Processing RX
- Green: JESD204B Interface

IQN

DDUC

Rx

(2) sets LVDS
JESD SYNCOUT
JESD SYSREF

Dual
JESD Lane
Parallel
Tx/Rx

Dual
JESD Lane
Parallel
Tx/Rx
Feedback Path

Color Legend
- JESD204B Interface
- DPD/Capture Buffer not be available on all devices

Stream Processing Feedback
# DFE Features (1)

<table>
<thead>
<tr>
<th>Key Features</th>
<th>Capacity</th>
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| Direct JESD204B connectivity with high speed data converters | • Four JESD204B TX and RX Serdes lanes, each supporting data rates up to 7.37Gbps  
• Two sets of JESD SYNC IN/OUT signals allow connection with up to two devices simultaneously |
| Number of Streams (Antennas)              | • Up to 4 transmit, 4 receive and 2 feedback streams (each RX and TX stream can be real or complex) |
| Number of Channels                        | • Four DDUCs (Digital Down/Up converters), each:  
• Supports up to 12 channels  
• Can be used for transmit or receive |
| Bandwidth Supported                       | • 368 MHz of instantaneous bandwidth  
• 150 MHz of occupied (processed) bandwidth  
• Fixed filters at the stream level provide 90% passband and 90dB stopband rejection |
# DFE Features (2)

<table>
<thead>
<tr>
<th>Transmit processing</th>
<th>Receive processing</th>
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<tbody>
<tr>
<td>• <strong>Channel processing</strong>: Filtering (programmable FIR filter), fractional re-sampling, frequency translation and summation (channel to stream conversion)</td>
<td>• <strong>Channel processing</strong>: Frequency translation, fractional re-sampling and filtering (programmable FIR filter)</td>
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<tr>
<td>• <strong>Stream processing</strong>: Fractional re-sampling, frequency translation (for low-IF support), JESD204B mapping and transport</td>
<td>• <strong>Stream processing</strong>: JESD204B transport and de-mapping, frequency translation (for low-IF support) and decimation</td>
</tr>
<tr>
<td>• Channel power meters for power monitoring</td>
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<tr>
<td>• Crest Factor Reduction (CFR)* and Digital Pre-Distortion (DPD)*</td>
<td>• Two feedback streams for TX monitoring (to support DPD*) or extra RX capacity</td>
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<tr>
<td>• TX signal processing bypass capability</td>
<td>• RX signal processing bypass capability</td>
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*Supported on K2L versions targeted towards wireless small cell base-station markets*
DFE System Use Cases

Typical DFE system use-case scenarios include:

- Discrete ADC and DAC
- Integrated RF Transceiver
- DFE Signal processing bypass
Use Cases: Discrete ADC and DAC (1)
Use Cases: Discrete ADC and DAC (2)

• Supported ADC classes:
  – RF Sampling: RF input/Complex output or Real input/Real output
  – Dual Real ADC (old technology): Complex input from IQ demodulator, Complex output
  – IF Sampling (Non zero-IF systems): Complex IF input, Complex output

• Supported DAC classes:
  – RF Sampling: Complex input, RF output (usually real)
  – Dual Real DAC (old technology): Complex input, Complex output at Zero-IF (for input to IQ modulator)
  – IF Sampling: Complex input, IF output (Real or Complex)
  – Single Real DAC: Real Input, Complex IF output
Use Cases: Integrated RF Transceiver

- Clock and SYSREF Solution
- RX
  - 2x JESD204B RX Lanes
- Feedback
  - 2x JESD204B RX Lanes
- Sync IN/Sync OUT

DUAL Tx/Rx, Feedback RF/JESD Transceiver

- Tx1
- Tx2
- Fb1
- Fb2
- Rx1
- Rx2
Use Cases: DFE Signal Processing Bypass
DFE Configuration

• The integrated DFE is configured using the RFSDK software provided by TI.
• RFSDK:
  – Runs on ARM/Linux
  – Uses TI-provided MCSDK Linux Dev Kit drivers to communicate with the hardware
  – Contains a set of pre-built radio configurations selectable by the customer
  – Provides set of APIs to start/stop operation and allow changing dynamic parameters (gain, etc.) during operation
  – Web server-based graphical interface for control and data visualization
• Data converters can also be configured from K2L device via I/O interfaces like SPI.
RFSDK Architecture

- RFSDK Radio Tools provide the top-level control interface.
- RFSDK Service performs actual control and configuration.
- Playback and Web Server provide RFSDK debug and test capabilities.
Get Started Today

Learn more:

- [66AK2Lx SoC Overview](#)
- [TI Design Page](#)
- [66AK2L06 Product Folder](#)
- [SYS/BIOS and Linux-MCSDK for Keystone-II Devices](#)