Optimization of Data Acquisition System

A detailed look at optimizing your input and reference drive circuits for lowest noise and distortion

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Agenda

• System Specification
• Theory of Operation
  – ADC Selection
  – Input Driver Design
  – Reference Driver Design
• Verification & Summary
• Appendix: Introduction to TI Design and Precision Labs
Agenda

• System Specification
  • Theory of Operation
    – ADC Selection
    – Input Driver Design
    – Reference Driver Design
• Verification & Summary
• Appendix: Introduction to TI Design and Precision Labs
“This is about the System, not the ADC”

• Customers often ask us why their SAR ADC is not performing to spec
  – ADC output not settling
  – Output is too noisy
  – Saturated output codes and behaving like a lower resolution device

• In most cases we find that customer’s input or reference drive circuits are unsuitable for their application => It’s about the system!

• Each application sets unique design goals
  – DC vs. AC performance
  – Performance vs. Power vs. Throughput

• SAR ADCs are highly versatile but to get the best out of a SAR ADC trade-offs must be made to optimize drivers for specific application
System Spec: Lowest Distortion and Noise @ 1MSPS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Goal (for 10KHz sine input)</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD</td>
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<td>+/-1.5LSB</td>
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<td>&lt; 40mW</td>
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• Theory of Operation
  – ADC Selection
  – Input Driver Design
  – Reference Driver Design

• Verification & Summary

• Appendix: Introduction of TI Design and Precision Labs
Theory of Operation

- Step 1: Choose the appropriate ADC that meets the system specification.
- Step 2: Select the proper input driving amplifier and charge bucket.
- Step 3: Design a high precision reference driver.

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Improving System Dynamic Performance

\[
\text{SINAD}_{\text{SYS}} = \frac{V_{\text{SIG,RMS}}}{\sqrt{V^2_{\text{n,TOT,RMS}} + V^2_{\text{HAR,TOT,RMS}}}}
\]

\[
V_{\text{HAR,TOT,RMS}} \approx \sqrt{V^2_{\text{HAR,ADC,RMS}} + V^2_{\text{HAR,INP,RMS}}}
\]

\[
V_{\text{n,TOT,RMS}} \approx \sqrt{V^2_{\text{n,ADC,RMS}} + V^2_{\text{n,INP,RMS}} + V^2_{\text{n,REF,RMS}}}
\]

To get maximum AC performance from the SAR ADC we need to minimize any degradation introduced by the driver circuits.

So we need:

\[
V_{\text{HAR,INP,RMS}} \ll V_{\text{HAR,ADC,RMS}}
\]

\[
V_{\text{n,INP,RMS}} \ll V_{\text{n,ADC,RMS}} \quad \text{and} \quad V_{\text{n,REF,RMS}} \ll V_{\text{n,ADC,RMS}}
\]
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## ADC Selection

### Parameter | Goal (for 10KHz sine input)
---|---
THD | < -110dB
SNR | > 98dB
INL | <+/-1.5LSB
Total Power | < 40mW

### Electrical Characteristics (continued)

All minimum and maximum specifications are at AVDD = 3 V, DVDD = 3 V, VREF = 5 V, VCM = VREF / 2 V, and fSAMPLE = 1 MSPS, over the operating free-air temperature range, unless otherwise noted. Typical specifications are at TA = 25°C, AVDD = 3 V, and DVDD = 3 V.

#### DYNAMIC CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>Signal-to-noise + distortion&lt;sup&gt;(6)&lt;/sup&gt;</td>
<td>At 1 kHz, VREF = 5 V</td>
<td>98</td>
<td>99.9</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At 10 kHz, VREF = 5 V</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At 100 kHz, VREF = 5 V</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio&lt;sup&gt;(6)&lt;/sup&gt;</td>
<td>At 1 kHz, VREF = 5 V</td>
<td>98.5</td>
<td>100</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At 10 kHz, VREF = 5 V</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At 100 kHz, VREF = 5 V</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion&lt;sup&gt;(6)(7)&lt;/sup&gt;</td>
<td>At 1 kHz, VREF = 5 V</td>
<td>-115</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At 10 kHz, VREF = 5 V</td>
<td>-112</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At 100 kHz, VREF = 5 V</td>
<td>-102</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

#### SYSTEM PERFORMANCE

<table>
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<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>RESOLUTION</th>
<th>UNIT</th>
</tr>
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<tbody>
<tr>
<td>Resolution</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>NMC</td>
<td>No missing codes</td>
<td>18</td>
<td>Bits</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential linearity</td>
<td>ADS8881C</td>
<td>-0.99</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADS8881I</td>
<td>-0.99</td>
</tr>
<tr>
<td>INL</td>
<td>Integral linearity&lt;sup&gt;(4)&lt;/sup&gt;</td>
<td>ADS8881C</td>
<td>-2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADS8881I</td>
<td>-3</td>
</tr>
<tr>
<td>Eo</td>
<td>Offset error&lt;sup&gt;(6)&lt;/sup&gt;</td>
<td></td>
<td>-4</td>
</tr>
<tr>
<td>PVa</td>
<td>Power dissipation</td>
<td>1-MHz sample rate, AVDD = 3 V</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100-kHz sample rate, AVDD = 3 V</td>
<td>0.55</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10-kHz sample rate, AVDD = 3 V</td>
<td>55</td>
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Requirement

- Drive a full-scale 10KHz sinusoidal signal across SAR ADC input sampling capacitor with minimal added distortion and noise
- Need 3 things from input driver
  1. Drive a cap load → low source impedance
  2. Low distortion → high Amp BW
  3. Low noise → low BW
- Opamp buffer requirements
  - Low THD
  - Low noise
  - Other: single 5V supply, RRO, low power
- Anti-aliasing filter requirements
  - Load Regulation
  - Must limit noise but not make opamp unstable
Selecting Amp for Low THD

- Need opamp with much lower distortion than ADC
  - \( \text{THD}_{\text{AMP}} < \text{THD}_{\text{ADC}} - 10\text{dB} = -120\text{dB} \)

- \( \text{THD}_{\text{AMP}} \) generally not a datasheet parameter so how do we pick low THD opamps?
  - Note: Do not use THD+N specification from datasheet for op amp THD
  - \( \text{THD}_{\text{AMP}} \) does not include the effect of noise

- Use GBW \( \rightarrow \) is specified in datasheet

- Opamps that have high GBW have low THD
  - Higher loop gain available over freq to correct for non-linearity

\[
V_{\text{OUT}}(f) = \frac{V_{\text{IN}}(f) \times A(f)}{1 + A(f)\beta(f)} + \frac{\text{NL}(f)}{1 + A\beta(f)}
\]

- \( \frac{\text{NL}}{1 + A\beta} \) is low as long as \( A\beta \) is high
Minimizing Input Buffer Distortion

- Short-list opamps with high GBW and compute $\text{THD}_{\text{AMP}}$ using dominant components specified on datasheet:
  - $\text{THD}_{\text{AMP}} = 10 \times \log\left(10^{\frac{HD_2}{10}} + 10^{\frac{HD_3}{10}}\right)$

- Inverting configuration better for THD
  - Opamps distort the output as inputs approach limits of input CM range
  - In non-inverting config $\text{Vin}+$, $\text{Vin}$- vary with the input signal → Common-mode distortion
  - Inverting config keeps opamp inputs fixed at $\text{Vin}- = \text{Vin}+ = \text{Vcm}$, which can be suitably chosen → No CM distortion
Input Driver Noise Contribution

- Dominated by the output-referred noise of the opamp buffer $V_{n\_AMP\_RTO\_RMS}$
- Need $V_{n\_AMP\_RTO\_RMS} < \frac{1}{5} \times V_{n\_ADC\_RMS} \approx 7\mu V$

$$2 \times NG \times V_{n\_AMP\_RTI\_RMS} < 7\mu V_{\text{rms}}$$

$$\sqrt{\left(\frac{\pi}{2} \times BW_{\text{FLT}} \times e^{2}_{n\_AMP}\right) + \left(\frac{\pi}{2} \times BW_{\text{FLT}} \times 4kT \frac{R}{2}\right)}$$

- $e_{n\_AMP}$ is a datasheet parameter
  - Solving inequality gives $e_{n\_AMP} < 5nV/\sqrt{Hz}$

$R_1 = R_2 = R$
Input Drive Amp Selection

Identify single +5V supply RRO opamp with:
1. THD < -120dB
2. Noise density $e_{n,AMP} < 5nV/\sqrt{Hz}$

<table>
<thead>
<tr>
<th>Op amp operated on single +5V supply</th>
<th>Output range [V]</th>
<th>GBW [MHz]</th>
<th>Calculated THD [dBc]</th>
<th>Noise [nV/rtHz]</th>
<th>Iq [mA]</th>
<th>Other</th>
</tr>
</thead>
<tbody>
<tr>
<td>THS4031</td>
<td>1.6 to 3.4</td>
<td>200</td>
<td>-</td>
<td>1.6</td>
<td>7.5</td>
<td>SE output</td>
</tr>
<tr>
<td>OPA2836</td>
<td>0.2 to 4.75</td>
<td>118</td>
<td>-132</td>
<td>4.6</td>
<td>1</td>
<td>SE output</td>
</tr>
<tr>
<td>THS4521</td>
<td>0.2 to 4.65</td>
<td>95</td>
<td>-132</td>
<td>4.6</td>
<td>1.14</td>
<td>Fully-diff output</td>
</tr>
<tr>
<td>THS4531</td>
<td>0.2 to 4.75</td>
<td>27</td>
<td>-121</td>
<td>10</td>
<td>0.25</td>
<td>Fully-diff output</td>
</tr>
</tbody>
</table>

THS4031 and OPA2836 meet the criteria for noise density.
Low-Distortion Anti-Aliasing Filter: $C_{FLT}$

- Anti-aliasing filter limits input path BW to $BW_{FLT} = \frac{1}{2\pi R_{FLT}(2C_{FLT})}$
- How to determine values of $C_{FLT}$, $R_{FLT}$?
  - Consider their alternate functions
- $C_{FLT}$ serves as “charge bucket” for charging $C_{SH}$ during sampling
  - $C_{SH}$ charges to $V_{FLT}$ and $C_{FLT}$ loses equivalent amount of charge $\Rightarrow V_{FLT}$ droops
  - Need $C_{FLT} \gg C_{SH}$ so droop is small
  - For droop of $\Delta V_{FLT} \leq 5\%V_{FLT}$ $C_{FLT} \geq 20 \times C_{SH} = 1.18nF$
- Larger $C_{FLT}$ also good for attenuating “kick-back” noise
- $C_{FLT}$ must be C0G/NP0 type for low THD $\Rightarrow$ typically <1uF
  - Stable capacitance over temp, freq, voltage

\[
C_{FLT} = \frac{1}{C_{cm}} + \frac{1}{2C_{cm}} \Rightarrow c_{cm} = 2C_{FLT}
\]

\[
Q_{SH} = \Delta Q_{FLT}
\]

$C_{SH} \times V_{FLT} = C_{FLT} \times \Delta V_{FLT} \leq C_{FLT} \times 0.05 \times V_{FLT}$

$C_{FLT} \geq 20 \times C_{SH}$
Low-Distortion Anti-Aliasing Filter: $C_{FLT}$

- Anti-aliasing filter limits input path BW to
  \[ BW_{FLT} = \frac{1}{2\pi R_{FLT}(2C_{FLT})} \]

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\[ Q_{SH} = \Delta Q_{FLT} \]
\[ C_{SH} \times V_{FLT} = C_{FLT} \times \Delta V_{FLT} \leq C_{FLT} \times 0.05 \times V_{FLT} \]
\[ C_{FLT} \geq 20 \times C_{SH} \]
Low-Distortion Anti-Aliasing Filter: $R_{FLT}$

- $C_{FLT}$ makes the opamp buffer unstable
  - Introduces low-freq pole at $\frac{1}{2\pi R_o C_{FLT}}$
  - AOL rolls off at -40dB/decade above pole freq and opamp runs out of PM

- Introducing $R_{FLT}$ stabilizes the opamp
  - Shifts pole to a lower freq and produces a zero
  - Pole degrades AOL phase but zero reverses it
  - AOL rolls off at -20dB/decade above $f_z$

- Need zero within 1 decade above pole for adequate phase margin

\[
f_z \leq 10 \times f_p \leq 10 \times \frac{1}{2\pi R_{FLT} C_{FLT}}
\]

\[
R_{FLT} \geq R_o/9
\]

- Need $R_{FLT} \leq R_{SWITCH}/10$ for low distortion
  - Voltage divider between $R_{FLT}$ and switch on-resistance attenuates input signal

\[
f_p = \frac{1}{2\pi(R_o + R_{FLT}) C_{FLT}} \quad f_z = \frac{1}{2\pi R_{FLT} C_{FLT}}
\]
Anti-aliasing Filter Components

- Need $C_{FLT} \geq 20 \times C_{SH}$
  - $C_{SH} = 59 pF \Rightarrow C_{FLT} \geq 1.18 nF$

- Need $\frac{R_o}{9} \leq R_{FLT} \leq \frac{R_{SWITCH}}{10}$
  - THS4521 $R_o$ calculated from plot
    - $R_o \approx 90 \Omega \Rightarrow \frac{R_o}{9} \approx 10 \Omega$
  - ADS8881 has $R_{SWITCH} = 96 \Omega$
  - Picking $R_{FLT} = 10 \Omega$ satisfies
    $\frac{R_o}{9} \leq R_{FLT} \leq \frac{R_{SWITCH}}{9.6}$

<table>
<thead>
<tr>
<th>$C_{FLT}$</th>
<th>10nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{FLT}$</td>
<td>10Ω</td>
</tr>
<tr>
<td>$BW_{FLT}$</td>
<td>800KHz</td>
</tr>
</tbody>
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$R_{o_{cl}}(f) = \frac{R_o}{1 + A_{ol}(f)} \Rightarrow R_{o_{cl}}(GBW) = \frac{R_o}{1 + A_{ol}(GBW)}$

$A_{ol}(GBW) = 0 dB = 1V/V$ and THS4521 $GBW = 95 MHz$

$R_o(95 MHz) = 2 \times R_{o_{cl}}(95 MHz) = 180 \Omega$ diff or 90Ω SE
Input Driver Simulation: Stability
Input Driver Simulation: Noise

\[ V_{n_{\text{RMS}}_{\text{ADC}}} = \frac{2 \times 4.5V}{2\sqrt{2}} \times 10^{-99} \approx 36uV_{\text{rms}} \]

\[ V_{n_{\text{RMS}}_{\text{Inp}}} \approx 37\% \times V_{n_{\text{RMS}}_{\text{ADC}}} \]
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**Requirement**

- **Accurate DC voltage** to ADC REF input that exhibits **minimal variation** with time and **fast load transients**
  1. Low offset
  2. Low drift, Low noise
  3. Low output impedance for load regulation

- **Signal chain:**
  - High precision voltage reference
  - Low noise, high precision, high speed opamp buffer
  - RC snubber network → provide low source impedance, preserves opamp BW and stability
Reference Driver Noise Contribution

Dominated by output noise of voltage reference

Need $V_{n_{REF\_RMS}} < \frac{V_{n_{ADC\_RMS}}}{3}$

$$\sqrt{V^2_{\frac{1}{f_{REF\_RMS}}} + V^2_{BB_{REF\_RMS}}} < \frac{1}{3} \times \frac{FSR}{2\sqrt{2}} \times 10^{\frac{-SNR(dB)}{20}}$$

Depends on BW of VREF output
Need to optimize BW for noise and settling
Settling $\rightarrow$ wasteful power consumption!

$$\sqrt{\left(\frac{V_{1/f_{REF\_pp}}}{6.6}\right)^2 + \left(e_{n_{REF}}\sqrt{f_{REF\_3dB} \times \frac{\pi}{2}}\right)^2} < 12uV$$

Datasheet param

Not in datasheet but $e_{n_{REF}} \propto (I_{Q_{REF}})^{-1/2}$

Identify voltage references with higher $I_{Q_{REF}}$ and solve for $f_{REF\_3dB}$
Voltage Reference and Filter Components

- Selected REF5045 w/ IQ = 1mA
  - High accuracy 4.5V ± 0.05% output
  - Very low temperature drift (3ppm/°C):
    - $I_{Q\_REF} = 1.0 \text{mA} \Rightarrow e_{n} \approx 223 nV/\sqrt{Hz}$
    - $V_{1/f\_REF\_pp} = 13.5 \mu V_{pp}$

- Solving inequality for $f_{REF\_3dB}$:
  \[
  f_{REF\_3dB} < 234.5 \text{Hz}
  \]

- Need $C_{REF\_FLT} > 100 nF$ to keep thermal noise below 0.2uVrms
  - Chose $C_{REF\_FLT} = 1 \mu F$

- $R_{REF\_FLT} > \frac{1}{2\pi \times f_{REF\_3dB} \times C_{REF\_FLT}} = 679 \Omega$
  - Chose $R_{REF\_FLT} = 1K \Omega$

\[
\sqrt{\left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2 + \left(e_{n\_REF} \sqrt{f_{REF\_3dB} \times \frac{\pi}{2}}\right)^2} < 12 \text{uV}
\]
Reference Driver Load Regulation

• SAR ADC has a capacitive DAC \( \Rightarrow \) creates changing cap load on the REF input during conversion
  – Large transient load currents (several mA) cause Vref to droop
  – Output errors occur if Vref error >1LSB when comparator makes bit decision
  – Vref driver needs to regulate dynamic load so that Vref error < 1LSB during conversion

Sources: Chris Hall & Bob Benjamin
Reference Driver Load Regulation

- $C_{BUF\_FLT}$ functions as near-ideal voltage source supplying most of the load current
  - $C_{BUF\_FLT}$ loses charge and voltage droops
  - Need $C_{BUF\_FLT}$ to be large enough to regulate $V_{ref}$ to $<1$LSB error

Total charge transferred to $REF$ input during conversion window $T_{CONV\_MAX}$:

$$Q_{REF} = T_{CONV\_MAX} \times l_{\_ref}$$

$C_{BUF\_FLT}$ supplies $>66\%$ of $Q_{REF}$ and drops by $\Delta V$ after $T_{CONV\_MAX}$

$$C_{BUF\_FLT} \times \Delta V > \frac{2}{3} \times Q_{REF}$$

Need $\Delta V < 1$LSB = \frac{FSR}{2^N}$

$$C_{BUF\_FLT} > \frac{2}{3} \times \frac{l_{\_ref} \times T_{CONV\_MAX} \times 2^N}{FSR}$$

Need $C_{BUF\_FLT} > 9.6\mu F$, chose $C_{BUF\_FLT} = 10\mu F$
Reference Buffer

• Need low output impedance over wide freq range + high accuracy
  – Need loop gain for low Zout ➔ need opamp with high GBW
  – Accuracy ➔ low offset, low offset drift, low noise density

• Can use OPA350 but consumes too much power for this design (IQ > 5mA)

• “Composite” amp config is power-efficient (IQ < 800uA)
  – THS4281: high speed, low accuracy
  – OPA333: low speed, high accuracy
  – OPA333 noisy but output is heavily filtered

• At DC the OPA corrects the THS output for offset and drift

• At AC the THS buffers the OPA output and provides good regulation against large high frequency load transients
Snubber Network

- $C_{BUF\_FLT}$ reduces stability of driving opamp

- Placing $R_{BUF\_FLT}$ between buffer out and REF input improves stability but cuts BW and increases output impedance

- “Snubber” configuration good for stability and settling response

- $R_{BUF\_FLT}$ value required for opamp stability determined via simulation
Snubber Resistor and Ref Buffer Stability

Select $R_{BUF\_FLT} = 0.25\Omega \Rightarrow 50 \text{ – } 60^\circ$ phase margin

Output settles to $<0.5\text{LSB (19-bit level)}$ in $604\text{ns}$
Reference Driver Noise Simulation

• Noise densities integrated over 1 decade above the BW of the reference path
  – BW = GBW of THS4281 buffer = 95MHz

• Simulated noise contribution of the REF driver appears to exceed total ADC RMS noise (~35\text{uVrms})
  – Macro-models are often conservative

• Build and bench test
PCB Layout Guidelines

- Minimize length of trace supplying ADC REF input
  - parasitic inductance can cause instability and settling issues
  - Minimizes EMI/RFI

- Keep components close together and close to the ADC

- Keep traces of differential signals as symmetrical as possible
  - Minimizes common-mode errors
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System Performance Verification: DC Noise

- First order check of board design
- Measure cumulative system noise referred to ADC input
  - Apply constant DC input to ADC and plot histogram of data from multiple conversions
- Histogram should be Gaussian
  - Non-Gaussian features $\rightarrow$ ADC DNL issues, power supply decoupling issues, poor grounding, layout issues
System Dynamic Performance

\[ THD = 10 \log \left(10^{-115/10} + 10^{-112.4/10}\right) = -110 dB \]
### Summary of System Performance

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<tr>
<td>INL</td>
<td>&lt;= +/-1.5LSB</td>
<td>&lt;= +/-1.5LSB</td>
</tr>
<tr>
<td>Total Power</td>
<td>&lt; 40mW</td>
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26-point INL for inputs between +/-4.45V
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Introduction to TI Precision Labs

TI Precision Labs

TI Precision Labs is the electronics industry’s first comprehensive online classroom for analog engineers. The on-demand curriculum pairs theory and applied lab exercises to deepen the technical expertise of experienced engineers and accelerate the development of those early in their career. This free modular curriculum includes over 30 hands-on trainings and lab videos, covering analog amplifier design considerations with online course work.

Learn more about the National Instruments VirtualBench™ and TI Precision Labs - Op Amps Hardware Evaluation Module used in the hands-on lab modules.

Download and install TINA-TI, the preferred simulator used exclusively with TI Precision Labs - Op Amps.

Download the Analog Engineer’s Pocket Reference e-Book.

Internet Explorer® users may experience issues viewing Precision Labs. We recommend using an alternative browser, such as Chrome™, Firefox® or Safari®.

- Introduction
- Input Voltage Offset (Vos) and Input Bias Current (Ib)
- Input and Output Limitations
- Bandwidth
- Slew Rate
- Noise
- Stability
- Electrostatic Discharge (ESD)
- Electrical Overstress (EOS)
Introduction to TI Precision Labs
Introduction to TI Design

- Design Article => Reduce the Design Timing Cost!!!
- Design File => Free!!!
  - TINA-TI Simulation
  - Schematic
  - PCB Layout (Gerber)
  - BOM
TI Precision Designs and Tools

- **18-Bit Data Acquisition (DAQ) Block Optimized for 1-μs Full-Scale Step Response** – SLAU512
- **18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power** – SLAU513
- **18-Bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power < 1mW** – SLAU514
- **18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Distortion and Noise** – SLAU515

**ADS8881 EVM – PDK (MMB0)**

**ADC-PRO**
The 4 Designs and Optimizations

• To illustrate how to achieve an optimal tradeoff of response time vs. performance vs. power consumption depending on application requirements

• 1-μs Full-Scale Step Response
  – OPA2350 input opamp
  – 8MHz anti-aliasing filter
  – REF5045+THS4281+OPA333 REF driver

• Lowest Distortion and Noise @ 1MSPS
  – THS4521 input opamp
  – 800KHz anti-aliasing filter
  – REF5045+THS4281+OPA333 REF driver

• Lowest Power @ 1MSPS
  – OPA2320 input opamp
  – 1.6MHz anti-aliasing filter
  – REF5045+THS4281+OPA333 REF driver

• Ultra Low Power @10KSPS
  – OPA2333 input opamp
  – 17KHz anti-aliasing filter
  – OPA313 REF driver
## Performance Comparison

<table>
<thead>
<tr>
<th>Optimization</th>
<th>Vref</th>
<th>Power</th>
<th>Effective Resolution</th>
<th>ENOB</th>
<th>SNR</th>
<th>Linearity</th>
<th>Response time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-μs Full-Scale Step Response</td>
<td>4.5</td>
<td>60mW</td>
<td>18</td>
<td>15.5</td>
<td>95dB</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>Lowest Distortion and Noise @ 1MSPS</td>
<td>4.5</td>
<td>40mW</td>
<td>18</td>
<td>16</td>
<td>99dB</td>
<td>Excellent</td>
<td>Fair</td>
</tr>
<tr>
<td>Lowest Power @ 1MSPS</td>
<td>4.5</td>
<td>30mW</td>
<td>18</td>
<td>16</td>
<td>99dB</td>
<td>Fair</td>
<td>Good</td>
</tr>
<tr>
<td>Ultra Low Power @ 10KSPS</td>
<td>2.5</td>
<td>0.6mW</td>
<td>17</td>
<td>14.6</td>
<td>92dB</td>
<td>Good</td>
<td>Poor</td>
</tr>
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Thank You & Questions

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