The Signal Chain

Analog to Digital Converter Types
The two most common ADC architectures include the Successive Approximation Register (SAR) and the Delta Sigma (ΔΣ).
Analog to Digital Converter
An ADC’s key task is to take analog signals and convert them to digital bits that can be read, processed or manipulated by a host processor, microcontroller or FPGA.
SAR & Delta Sigma ADC Architectures

- SAR
- Delta Sigma

Converter Resolution (bits) vs. Sampling Rate (SPS)

- SAR
- Delta Sigma

- 8
- 12
- 16
- 20
- 24
- 28
- 32

- 10
- 100
- 1K
- 10K
- 100K
- 1M
- 10M
- 100M
SAR & Delta Sigma ADC Architectures

- **Converter Resolution (bits)**: 8, 12, 16, 20, 24, 32
- **Sampling Rate (SPS)**: 10, 100, 1K, 10K, 100K, 1M, 10M, 100M

**Delta Sigma**

**SAR**
SAR & Delta Sigma ADC Architectures

Converter Resolution (bits) vs. Sampling Rate (SPS)

- **SAR**
  - 8 to 12 bits
  - Sampling Rates: 10 - 100 MSPS

- **Delta Sigma**
  - 16 to 32 bits
  - Sampling Rates: 1K - 100 MSPS

Texas Instruments
More Precision ADC Information

PA SAR ADC Web Page: www.ti.com/precisionadc
- Data Sheets & Technical Reference Manuals
- Application Notes
- Software, Tools & SPICE Model Downloads
- Order Evaluation & Performance Demonstration Kits

PA SAR ADC E2E™ Support Forum: www.ti.com/precisionadcsupport
- Ask Technical Questions
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Precision HUB Blog Series: e2e.ti.com/blogs_/b/precisionhub
   Tips, tricks and techniques from TI precision analog experts

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