KeyStone II
ARM Cortex-A15
CorePac Overview
ARM A15 CorePac in KeyStone II

Standard ARM Cortex-A15 MPCore processor
- Cortex-A15 MPCore version r2p2
- Quad-core, dual-core, and single-core variants
- 4096kB L2 cache
  - 20cc L1 miss L2 hit load to use
  - Same latency on dual and single core variants
- Per core NEON (SIMD co-processor)
  - 128-bit wide SIMDv2 processor
  - 8, 16, 32, and 64-bit data types
  - Single-precision floating point
- Per core VFP (vector floating point co-processor)
  - Single and double-precision floating point, VFPv4
- Error correction and detection on L1 and L2 caches
- AXI-4 ACE interface for cache coherent interconnect
- GIC-400 Interrupt Controller (SoC level)
Each Cortex-A15 Core in the MPCore

- Full ARMv7-A architecture instruction set
- 3-issue out-of-order pipeline (3-12 stages)
- Dynamic branch prediction
  - 2k entry Branch Target Buffer (BTB), 8k entry Global History Buffer (GHB)
- 32kB data L1 cache and 32kB L1 instruction cache
  - 4cc load to use latency (typically hidden by out-of-order pipeline)
- Full support for virtualization, 32bit virtual and 40bit physical addresses
  - 2-level Memory Management unit (MMU)
    - Virtual to intermediate physical address
    - Intermediate physical to physical address
  - Three 32-entry fully associative L1 TLBs
    - Instruction fetch, load, store
  - 512-entry 4-way set associative L2 TLB
- Performance Monitoring Unit (6 counter PMUv2)
KeyStone II Quad Cortex-A15 MPCore

ARM Cortex-A15 MPCore

ARM GIC-400 interrupt controller

Access to and from the SoC
KeyStone II ARM CorePac: Key Features

• Cache coherency for ARM CorePac and IO
  – ARM CorePac and DDR3 (DDR3A for those devices with multiple DDR3s)
  – MSMC SRAM (on-chip scratch memory)
• Low latency and high bandwidth connection from CorePac to external memory
• Virtualization support with 40-bit physical addressing (large physical address extensions, LPAE)
• Large L2 cache (4MB, 16-way set associative)
• Reliability and availability with ECC in internal and external memories
• High-performance IO from user space and any paravirtualized guest OS
• Energy efficiency
KeyStone II: IO Cache Coherency

- IO Coherency for the ARM, SMP for the quad cluster
  - DDR3A from 0x08_0000_0000 to 0x09_FFFF_FFFF
  - MSMC SRAM
- Coherency for ease of use and performance
Benchmarks: Core Only, Memory Latency

- Dhrystone, DMIPS/MHz, CPU core and L1 only
  - 3.5DMIPS/MHz (highly dependant on compiler)
  - 19600DMIPS with KeyStone II Quad-ARM CorePac at 1.4GHz
- Floating point
  - Quad single-precision IEEE-754 FMAC per cycle
- Memory Latency, load-to-use latency
  - 4cc L1D hit, typically hidden by A15 micro architecture
  - 20cc L2 hit (4MB)
  - MSMC2 SRAM: ~50cc
  - External Memory: ~100ns L2 miss to DDR page that is open
Memory Bandwidth Benchmarks

DDR3-1600 theoretical throughput 12.8GB/s

~30% to ~50% achieved

Physical placement of arrays is critical; Linux virtual memory with 4kB pages is good.

Memory Bandwidth, external memory only:

- Stream Copy \( a(i) = b(i) \), where \( a \) and \( b \) are arrays.
- Stream Scale \( a(i) = q \times b(i) \), where \( a \) and \( b \) are arrays, and \( q \) is a constant.
- Stream Add computes \( a(i) = b(i) + c(i) \), where \( a, b, \) and \( c \) are arrays.
- Stream Triad computes \( a(i) = b(i) + q \times c(i) \), where \( a, b, \) and \( c \) are arrays, and \( q \) is a constant.
- Array sizes are defined to force missing on cache regardless of size
Virtualization

- Long-descriptor format page tables
  - 40-bit physical addressing (LPAE)
  - Short-descriptor with 32-bit physical addressing with ARM CorePac running from DDR3B
- Three-level data structure to get to 4kB pages at each stage
  - Two levels to get to 2MB pages (Linux huge pages)
  - TLBs cache a page per entry
- Hypervisor privilege (3rd level, user, supervisor)
  - Manages the second-stage address translation per each virtual machine
  - HW traps exceptions, CP15 register access and WFI/WFE
- Paravirtualized drivers or direct IO register access for IO performance
- IO accesses use MPAX
Reliability

• KeyStone II ARM CorePac is designed for high-reliability embedded applications.
  – 100k power on hours at 105C
• Data caches support SECDED (single-bit error correct, double-bit error detect).
  – L1D and L2 caches data and tag RAMs
• Program caches support parity and refetch on error.
  – L1I cache
  – Tag RAM
  – Branch Target Buffer (BTB)
Energy Efficiency

• Clock gating inside the ARM CorePac:
  – Total dynamic power consumption for a fully-loaded 1.4GHz core will range from 1.2W to 0.35W depending on the type of instructions it runs.
  – Wait for interrupt and event (WFI, WFE) instructions bring the dynamic power down to <0.1W per core.

• Power switches per core and per quad cluster including L2:
  – Each ARM A15 core can be shut down independently
  – The entire Quad-ARM A15 CorePac, including the 4MB/1MB L2 cache, can also be shut down.
  – Reduces static power to <5%
KeyStone II Architecture

- Memory Subsystem
  - 72-Bit DDR3a EMIF
  - 72-Bit DDR3b EMIF
- Debug & Trace
  - ARM Boot ROM
  - Semaphore
  - Secure Mode
  - Power Management
  - PLL
  - EDMA
- Miscellaneous
- HyperLink
- TeraNet
- Multicore Navigator
  - Queue Manager
  - Packet DMA
- Device-Specific
  - EMIF 16
  - GPIO x 32
  - I²C x 3
  - USB 3.0 x 2
  - UART x 2
  - SPI x 3
  - PCIe x 2
  - SRI x 4
- 3-Port Ethernet Switch
  - 10GBE
- 5-Port Ethernet Switch
  - 10GBE
- Network Coprocessor
- Security Accelerator
- Packet Accelerator

1-4 ARM Cores & 1-8 DSP Cores @ up to 1.4 GHz
For More Information

• ARM Reference Manuals
  http://infocenter.arm.com/help/index.jsp
  – A15 Technical Reference Manual (TRM) r2p2
  – GIC-400 r0p0rel1

• STREAM Benchmark
  http://www.cs.virginia.edu/stream/

• For questions regarding topics covered in this training, visit the support forums at the TI E2E Community website.

• KeyStone SoC & Software Overview Training