KeyStone II SoC Overview

Multicore Applications
KeyStone II SoC Overview

• KeyStone II Architecture
• CorePacs & Memory Subsystem
• Multicore Navigator
• Interfaces and Peripherals
• Debug
• Platform-Specific Device Variations
• KeyStone I to KeyStone II Comparison
KeyStone I Device Architecture
KeyStone II Device Architecture

- C66x CorePac
- ARM A15 CorePac
- Memory Subsystem
- Multicore Navigator
- Network Coprocessor
- TeraNet Switch Fabric
- 10 Gigabit Ethernet (10 GBE)
- External Interfaces
- HyperLink Bus
- Miscellaneous
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C66x CorePac

- 0-8x C66x CorePac(s) operating at up to 1.25 GHz.
  - Fixed- and floating-point operations
  - Code compatible with other C64x+ and C67x+ devices
- L1 Memory
  - Can be partitioned as cache and/or RAM
  - 32KB L1P per core
  - 32KB L1D per core
  - Error detection for L1P
  - Memory protection
- Dedicated L2 Memory
  - Can be partitioned as cache and/or RAM
  - 1 MB Local L2 per core
  - Error detection and correction for all L2 memory
- Direct connection to memory subsystem
- Direct connection to Teranet switch fabric.
ARM Cortex-A15 CorePac

- Single, Dual, or Quad-ARM A15 CorePac operating at up to 1.4 GHz.
  - Full implementation of ARMv7-A architecture instruction set
  - Integrated Neon and Vector Floating-Point Unit

- L1 Memory: 32KB L1 per ARM A15 for caching program and data

- L2 Memory:
  - Shared L2 Cache Memory with full cache coherency using Snoop Control Unit (SCU)
  - 4 MB L2 Cache is shared between the 1 to 4 ARM A15 core(s).

- AMBA 4.0 AXI Coherency Extension (ACE) master port connected directly to the MSMC2 for short-path access to shared MSMC SRAM

- The ACE also provides an IO coherent access to the shared memory and external memory connected through the EMIF interface.

- Cluster-level and core-level power management and low-power standby modes (also known as WFI/WFE modes)
Memory Subsystem: MSM/MSMC

- **Multicore Shared Memory (MSM SRAM)**
  - 2-6 MB shared among the C66x and ARM A15 CorePacs.
  - May contain program and data

- **Multicore Shared Memory Controller (MSMC version 2.0)**
  - Arbitrates access of C66x and ARM A15 CorePac and SoC masters to shared and external memory through DDR3 EMIF
  - Provides error detection and correction for all shared memory
  - Memory protection and address extension to 64 GB (36 bits)
  - Provides multi-stream pre-fetching capability
  - Support for ARM coherency with EDMA/peripheral masters in DDR3A and MSMC SRAM space.
  - 8 SRAM banks
  - Runs at the DSP frequency, thereby increasing memory access by fourfold compared to previous MSMC version 1.0
Memory Subsystem: DDR3

Up to two DDR3 subsystem(s) per device:

• The first DDR3 subsystem (DDR3A) supports up to 8 GB memory addresses and is connected to the CorePac(s) through the MSMC.

• When present, the second DDR3 subsystem (DDR3B) supports up to 2 GB memory address and is connected directly to the TeraNet.

• Each DDR consists of a 64b/72b EMIF controller:
  – Supports 16-bit, 32-bit, and 64-bit modes.
  – Operates at up to 1600 MT/s
  – Supports power down of unused pins when using 16-bit or 32-bit width
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Multicore Navigator

- Consists of the following:
  - 1-2x Queue Manager.
  - Multiple, dedicated Packet DMA engines
  - 1-2x infrastructure DMAs
- Provides seamless inter-core communications (messages and data exchanges) between cores, IP, and peripherals. “Fire and forget.”
- Low-overhead processing and routing of packet traffic to and from peripherals and cores
- Supports dynamic load optimization
- Data transfer architecture designed to minimize host interaction while maximizing memory and bus efficiency
- Supports up to 8K or 16K hardware queues and 512K to 1M descriptors.
Multicore Navigator Architecture

TeraNet

PKTDMA

QM1
Link RAM
PKTDMA

QM2
PKTDMA
PDSP 1 - 8
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Network Coprocessor

- Consists of 1-2x Network Coprocessor
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple queues
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols
- 1-2x 5-port Ethernet switches (depending on number of instances of NetCp) with 4-8 ports connecting to 4-8 SGMII ports and one port connecting to the Packet and Security Accelerators.
External Interfaces

- 4-8x SGMII ports support 10/100/1000M Ethernet through 1-2x 5-port Ethernet switch(es).
- 2x XGMII ports support up to 10G Ethernet through a 3-port Ethernet switch.
- 4x high-bandwidth Serial RapidIO (SRIO v2.1) lanes for inter-DSP applications.
- 1-2x PCIe at 5 Gbps
- 3x SPI modules with up to four chip selects per module.
- 2x UART for development/testing
- 1-2x USB 3.0
- 3x I2C at 400 Kbps
- 32 GPIO pins
- EMIF 16
- Device-specific interfaces
HyperLink Bus

- Provides TI-propriety, high-speed interconnects termed HyperLink.
- Up to 2x HyperLink modules with 4 lanes each.
- Provides the capability to expand the device to include hardware acceleration or other auxiliary processors.
- Supports up to 12.5 Gbaud per lane.
TeraNet Switch Fabric

- A non-blocking switch fabric that enables contention-free internal data movement at a high rate of 2 Tbps
- Provides a configured way – within hardware – to manage traffic queues and ensure priority jobs are getting accomplished while minimizing the involvement of the CorePac cores
- Facilitates high-bandwidth communications between CorePac cores, subsystems, peripherals, and memory
• ARM- and DSP-driven Boot ROM:
  - C66x CorePacs support booting from SRIO, PCIe, I2C Master, I2C Slave, SPI, Ethernet, XIP, and HyperLink.
  - ARM CorePacs support booting from UART, NAND, XIP, SPI, Ethernet, PCIe, I2C, SRIO and HyperLink.
  - Support varies by peripheral availability
• Semaphore module provides atomic access to shared chip-level resources.
• Secure Mode
• Power Management:
  - Manages power- and clock-switching of individual IPs and CorePac(s).
  - Supports Dynamic Power Switching (DPS):
    • Power state hibernation modes 1 and 2
    • Manages each C66x CorePac, each ARM core, and/or the entire ARM CorePac
    • Reset isolation capability on select peripherals
    • SmartReflex Class 0 and Class 3
• Up to 5 on-chip PLLs:
  - One Main PLL
  - One PLL for DDR3A
  - One PLL for DDR3B
  - One PLL for ARM CorePac
  - One PLL for Packet Accelerator
• 5x EDMA controllers
• 20 64-bit timers
• Inter-Processor Communication (IPC) Registers
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Diagnostic Enhancements

- Embedded Trace Buffers (ETB) enhance the diagnostic capabilities of the CorePac.
- CP Monitor enables diagnostic capabilities on data traffic through the TeraNet switch fabric.
- Automatic statistics collection and exporting (non-intrusive).
- Monitor individual events for better debugging.
- Monitor transactions to both memory endpoint and Memory-Mapped Registers (MMR).
- Configurable monitor filtering capability based on address and transaction type.
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KeyStone II Part Numbering

PREFIX
- X = Experimental device
- Blank = Qualified device

DEVICE FAMILY
- 66A = DSP + ARM SoC

ARCHITECTURE
- K2 = KeyStone II

PLATFORM
- H

DEVICE NUMBER
- 12

SILICON REVISION
- Blank = Initial 1.0 silicon

DEVICE SPEED RANGE
- Blank = 1 GHz
- 2 = 1.2 GHz

TEMPERATURE RANGE
- Blank = 0°C to +100°C (default core temperature)
- A = Extended temperature range
  -40°C to 100°C

PACKAGE TYPE
- AAW = 1517-pin plastic ball grid array, with Pb-free solder balls and die bumps

SECURITY
- Blank = No Security Accelerator / No SOC security
- X = Security Accelerator enabled
- D = Security Accelerator and SOC security enabled with 11 development keys
- S = Security Accelerator and SOC security enabled with production keys
## K2H Compared to K2E

<table>
<thead>
<tr>
<th>Platform</th>
<th>C66x DSP</th>
<th>ARM A15</th>
<th>Max Clock Ghz</th>
<th>MSMC Shared Memory – MB</th>
<th>Navigator Queues</th>
<th>DDR3 EMIF 72-bit 1600 MTP/s</th>
<th>5-Port 1GB Switch</th>
<th>3-Port 10GB Switch</th>
<th>USB 3.0</th>
<th>Hyperlink</th>
<th>SRI0 x4</th>
<th>PCIe x2</th>
<th>TSIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>K2E</td>
<td>0x to 1x</td>
<td>1x to 4x</td>
<td>ARM = 1.4</td>
<td>2</td>
<td>8K</td>
<td>1x</td>
<td>1x to 2x</td>
<td>2x</td>
<td>2x</td>
<td>1x</td>
<td>--</td>
<td>2x</td>
<td>1x</td>
</tr>
<tr>
<td>K2H</td>
<td>4x to 8x</td>
<td>2x to 4x</td>
<td>ARM = 1.4</td>
<td>6</td>
<td>16K</td>
<td>2x</td>
<td>1x</td>
<td>--</td>
<td>1x</td>
<td>2x</td>
<td>1x</td>
<td>1x</td>
<td>--</td>
</tr>
</tbody>
</table>
The K2H platform has two variations:

- **66AK2H12**
  - 8x C66x CorePacs
  - Quad-ARM A15 CorePac
  - 2x Queue Managers support up to 16K queues
  - 1x Network Coprocessor
  - 1x USB3.0 to support solid state drive
  - 10GBE interface is NOT available.
The K2H platform has two variations:

- **66AK2H12**
  - 8x C66x CorePacs
  - Quad-ARM A15 CorePac
  - 2x Queue Managers support up 16K queues
  - 1x Network Coprocessor
  - 1x USB3.0 to support solid state drive
  - 10GBe interface is NOT available

- **66AK2H06**
  - Scaled-down version of 66AK2H12
  - 4x C66x CorePacs
  - Dual-ARM A15 CorePac
The K2E platform has four variations:

- **AM5K2E04**
  - First ARM-only multicore device from TI
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up 8K queues
  - 2x Network Coprocessor
  - 1x 3 port 10GBE Switch Subsystem
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO
The K2E platform has four variations:

- **AM5K2E04**
  - First ARM-only multicore device from TI
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up to 8K queues
  - 2x Network Coprocessor
  - 1x 3 port 10GBE Switch Subsystem
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO

- **AM5K2E02**
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 1x Network Coprocessor
  - 10GBE not included
The K2E platform has four variations:

- **AM5K2E04**
  - First ARM-only multicore device from TI
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up 8K queues
  - 2x Network Coprocessor
  - 1x 3 port 10GBE Switch Subsystem
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO

- **AM5K2E02**
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 1x Network Coprocessor
  - 10GBE not included

- **66AK2E05**
  - Same as AM5K2E04 with 4x PLL and a single C66x CorePac added

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The diagram illustrates the detailed architecture of the K2E platform, showing various components such as the C66x™ CorePac, Network Coprocessor, and various memory and interface subsystems. Each variation is represented with specific configuration details provided in the text.
The K2E platform has four variations:

- **AM5K2E04**
  - First ARM-only multicore device from TI
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up 8K queues
  - 2x Network Coprocessor
  - 1x 3 port 10GBE Switch Subsystem
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
    - No SRIO

- **AM5K2E02**
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 1x Network Coprocessor
  - 10GBE not included

- **66AK2E05**
  - Same as AM5K2E04 with 4x PLL and a single C66x CorePac added

- **66AK2E02**
  - Same as AM5K2E02 with 4x PLL and a single-ARM A15 CorePac and a single C66x CorePac added
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## KeyStone I Compared to KeyStone II

<table>
<thead>
<tr>
<th>IP block</th>
<th>KeyStone I</th>
<th>KeyStone II</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM Cortex-A15 core</td>
<td>No</td>
<td>4x</td>
</tr>
<tr>
<td>MSMC</td>
<td>Ver1.0</td>
<td>Ver2.0</td>
</tr>
<tr>
<td>DDR3 EMIF (64-bit)</td>
<td>1x</td>
<td>2x</td>
</tr>
<tr>
<td>MSMC SRAM</td>
<td>2 Mbytes</td>
<td>6 Mbytes</td>
</tr>
<tr>
<td>DDR3A memory (max)</td>
<td>8 Gbytes</td>
<td>8 Gbytes</td>
</tr>
<tr>
<td>DDR3B memory (max)</td>
<td>No</td>
<td>2 Gbytes (for ARM and DSP cores)</td>
</tr>
<tr>
<td>ARM Boot ROM</td>
<td>No</td>
<td>256 Kbytes</td>
</tr>
<tr>
<td>OTP memory</td>
<td>No</td>
<td>4 Kbits</td>
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<tr>
<td>Queue Manager Subsystem + PKTDMA</td>
<td>1x</td>
<td>2x</td>
</tr>
<tr>
<td>EDMA3CC</td>
<td>3x</td>
<td>5x</td>
</tr>
<tr>
<td>EDMA3TC</td>
<td>10x</td>
<td>14x</td>
</tr>
<tr>
<td>HyperLink</td>
<td>1 x 4</td>
<td>2 x 4</td>
</tr>
<tr>
<td>10 Gigabit Ethernet (10GBE)</td>
<td>No</td>
<td>1 x 2</td>
</tr>
<tr>
<td>UART</td>
<td>1x</td>
<td>2x</td>
</tr>
<tr>
<td>SPI</td>
<td>1x</td>
<td>3x</td>
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<tr>
<td>I2C</td>
<td>1x</td>
<td>3x</td>
</tr>
<tr>
<td>GPIO</td>
<td>1x 16</td>
<td>1x 32</td>
</tr>
<tr>
<td>Timer64</td>
<td>8x</td>
<td>20x</td>
</tr>
<tr>
<td>USB3</td>
<td>No</td>
<td>1x to 3x</td>
</tr>
<tr>
<td>PLL controller + On-chip PLLs</td>
<td>3x</td>
<td>5x</td>
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<tr>
<td>ARM Subsystem ETB (16 KB)</td>
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<td>DSP TETB (4 KB)</td>
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</tr>
<tr>
<td>Tracer</td>
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<td>32x</td>
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<tr>
<td>MPU</td>
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<td>15x</td>
</tr>
<tr>
<td>Security Manager</td>
<td>No</td>
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</tr>
</tbody>
</table>
For More Information

- Device-specific Data Manuals for the KeyStone II SoCs can be found at [TI.com/multicore](http://TI.com/multicore).
- Multicore articles, tools, and software are available at [Embedded Processors Wiki for the KeyStone Device Architecture](http://Embedded Processors Wiki for the KeyStone Device Architecture).
- For questions regarding topics covered in this training, visit the support forums at the [TI E2E Community](http://TI E2E Community) website.