# KeyStone Training

# Power Management



# Agenda

- Overview
- Power Domains
- Clock Domains
- Power States
- SmartReflex

# C66x Power Overview

- Overview
- Power Domains
- Clock Domains
- Power States
- SmartReflex



# New Power Management Features

New features:

– Switchable Logic and Memory Power Domains

– Various Power States

– SmartReflex Class 3

# Power Domains

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- Power Domains
- Clock Domains
- Power States
- SmartReflex



# Power Domain Topology

- The GPSC manages each of the power domains , allowing any to be independently switched off of the power grid, removing all of the clocking and leakage power contribution by that block . Some power domains will be used to control sleep for memories within each power domain.
- One power domain can have one or more clock domains.
- Clock gating to each of the logic blocks is managed by the LPSCs of each module.

# Power Domains: KeyStone Media Applications

| Domain | Block | Note | Power Connection | Default State |
|---|---|---|---|---|
| 0 PD_ALWAYSON | SmartReflex IPs, MSMC, Some peripheral logic | Cannot be disabled | Always on | ON |
| 1 PD_DEBUG_TRC (RAM_PSM) | TETB RAMs | RAMs can be turned into OFF-Mode | Software control | OFF |
| 2 PD_NETCP | NETCP + CPGMAC_x2+SRAM | NETCP+CPGMAC_x2 (sgmii) Logic+SRAM can be powered down. | Software control | OFF |
| 3 PD_PCIEX | PCIe Logic+SRAM | PCIe Logic+SRAM can be powered down SW control | BOOTSTRAP Pin: PCIESSEN | |
| 4 PD_SRIO | SRIO Logic +SRAM | SRIO Logic+SRAM can be powered down | Software control | OFF |
| 5 PD_HyperLink | HyperLink Logic+SRAM | HyperLink Logic+SRAM can be powered down | Software control | OFF |
| 6 Reserved | | | | |
| 7 PD_MSMCSRAM (RAM_PSM) | MSMCSRAM | RAMs can be turned into OFF-Mode | Software control | ON |
| 8 PD_CorePac0 | CorePac0 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 9 PD_CorePac1 | CorePac1 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 10 PD_CorePac2 | CorePac2 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 11 PD_CorePac3 | CorePac3 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 12 PD_CorePac4 | CorePac4 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 13 PD_CorePac5 | CorePac5 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 14 PD_CorePac6 | CorePac6 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 15 PD_CorePac7 | CorePac7 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |



# Power Domains: KeyStone Wireless Applications

| Domain | Block(s) | Note | Power connection | Default State |
|---|---|---|---|---|
| 0 PD_ALWAYSON | SmartRflex IPs, MSMC | Cannot be disabled | Always on | ON |
| 1 PD_DEBUG_TRC(RAM_PSM) | TETB RAMs | RAMs can be turned into OFF-Mode | Software control | OFF |
| 2 PD_NETCP | NETCP + CPGMAC_x2 Logic+SRAM | NETCP + CPGMAC_x2 Logic+SRAM can be powered down | Software control | OFF |
| 3 PD_PCIEX | PCIe Logic+SRAM | PCIe Logic+SRAM can be powered down | Software control | BOOTSTRAP PIN: PCIESSEN |
| 4 PD_SRIO | SRIO Logic+SRAM | SRIO Logic+SRAM can be powered down | Software control | OFF |
| 5 PD_HyperLink | HyperLink Logic+SRAM | HyperLink Logic+SRAM can be powered down | Software control | OFF |
| 6 Reserved | | | | |
| 7 PD_MSMCSRAM (RAM_PSM) | MSMCSRAM | RAMs can be turned into OFF-Mode | Software control | ON |
| 8 PD_RAC_TAC | RAC_A +RAC_B + TAC | RAC_A +RAC_B +TAC can be powered down | Software control | OFF |
| 9 PD_FFTC | FFTC | FFTC can be powered down | Software control | OFF |
| 10 PD_AI (RAM_PSM) | AIF2 SRAM | RAMs can be turned into OFF-Mode | Software control | OFF |
| 11 PD_TCP3D (RAM_PSM) | TCP3d SRAM | RAMs can be turned into OFF-Mode | Software control | OFF |
| 12 PD_VCP_BCD (RAM_PSM) | VCP2-B/C/D SRAM | RAMs can be turned into OFF-Mode | Software control | OFF |
| 13 PD_CorePac0 | CorePac0 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |
| 14 PD_CorePac1 | CorePac1 RAMs + RSA_1_A/B | Only L1,L2 and other CorePac memory+RSA logic | Software control | ON |
| 15 PD_CorePac2 | CorePac2 RAMs + RSA_2_A/B | Only L1,L2 and other CorePac memory+RSA logic | Software control | ON |
| 16 PD_CorePac3 | CorePac3 RAMs | Only L1,L2 and other CorePac memory | Software control | ON |

# Clock Domains

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# Clock Domains: KeyStone Media Applications

| LPSC# | Module(s) | RESET_ISO (1 indicates capable of being reset isolated) | Notes | Power Domain Number |
|---|---|---|---|---|
| 0 | | | | |
| MOD_MODRST0 | Shared LPSC - For all modules other than listed in this table. | 0 | Always on | 0 |
| 1 | | | | |
| MOD_SRc3_PWR | SmartRflex3 | 1 | Always on | 0 |
| 2 | | | | |
| MOD_EMIF4F | DDR3 EMIF | 0 | Software control | 0 |
| 3 | | | | |
| MOD_EMIFA_SPI | EMIFA/SPI | 0 | Software control | 0 |
| 4 | | | | |
| MOD_TSIP | TSIP | 0 | Software control | 0 |
| 5 | | | | |
| MOD_DEBUGSS_TRC | DEBUGSS+CP_TRACER+Local SCR | 1 (only STM and ETB are reset isolated) | Software control | 1 |
| 6 | | | | |
| MOD_TETB_TRC | TETBs | 1 | Software control | 1 |
| 7 | | | | |
| MOD_PKTPROC | NETCP Packet Accelerator | 0 | Software control | 2 |
| 8 | | | | |
| MOD_CPGMAC | NETCP CPGMACs | 1 | Software control | 2 |
| 9 | | | | |
| MOD_SA | PA_SS SA | 0 | Software control | 2 |
| 10 | | | | |
| MOD_PCIEX | PCIe | 0 | Software control | 3 |
| 11 | | | | |
| MOD_SRIO | SRIO | 1 | Software control | 4 |

# Clock Domains: KeyStone Media Applications

| | | | | | |
|---|---|---|---|---|---|
| 12 | | | | | |
| MOD_HyperLink | HyperLink | 0 | Software control | 5 | |
| 13 | | | | | |
| MOD_L2SRAM | L2SRAM | 0 | Software control | 6 | |
| 14 | | | | | |
| MOD_MSMCSRAM | MSMCSRAM | 0 | Software control | 7 | |
| 15 | | | | | |
| MOD_CorePac0 | CorePac0+local timer | 0 | Software control | 8 | |
| 16 | | | | | |
| MOD_CorePac1 | CorePac1+local timer | 0 | Software control | 9 | |
| 17 | | | | | |
| MOD_CorePac2 | CorePac2+local timer | 0 | Software control | 10 | |
| 18 | | | | | |
| MOD_CorePac3 | CorePac3+local timer | 0 | Software control | 11 | |
| 19 | | | | | |
| MOD_CorePac4 | CorePac4+local timer | 0 | Software control | 12 | |
| 20 | | | | | |
| MOD_CorePac5 | CorePac5+local timer | 0 | Software control | 13 | |
| 21 | | | | | |
| MOD_CorePac6 | CorePac6+local timer | 0 | Software control | 14 | |
| 22 | | | | | |
| MOD_CorePac7 | CorePac7+local timer | 0 | Software control | 15 | |
| No LPSC | Bootcfg, PSC, Main PLLCTL. | | These modules do not use LPSC. | 0 | |

NOTE: For an IP to be reset isolated, reset isolation needs to be enabled by configuration of one MMR (RESETISO in Module Control Register) in the corresponding LPSC. Boot ROM code configures the MMR to enable reset isolation for SmartReflex, SRIO and SGMII.



# Clock Domains: KeyStone Wireless Applications

| LPSC# | Modules | RESET_ISO (1 indicates capable of being reset isolated) | | | Power Domain Number |
|---|---|---|---|---|---|
| 0 | | | | | |
| MOD_MODRST0 | Shared LPSC - For all modules other than listed in this table. | | 0 | Always on | 0 |
| 1 | | | | | |
| MOD_SRc3_PWR | SmartRflex3 | | 1 | Always on | 0 |
| 2 | | | | | |
| MOD_EMIF4F | DDR3 EMIF | | 0 | Software control | 0 |
| 3 | | | | | |
| MOD_TCP3E | TCP3e | | 0 | Software control | 0 |
| 4 | | | | | |
| MOD_VCP2_A | VCP2_A | | 0 | Software control | 0 |
| 5 | | | | | |
| MOD_DEBUGSS_TRC | DEBUGSS+CP_TRACER+Local SCR | 1(only STM and ETB are reset isolated) | | Software control | 1 |
| 6 | | | | | |
| MOD_TETB_TRC | TETBs | | 1 | Software control | 1 |
| 7 | | | | | |
| MOD_PKTPROC | NETCP Packet Accelerator | | 0 | Software control | 2 |
| 8 | | | | | |
| MOD_CPGMAC | NETCP CPGMACs | | 1 | Software control | 2 |
| 9 | | | | | |
| MOD_SA | NETCP SA | | 0 | Software control | 2 |
| 10 | | | | | |
| MOD_PCIEX | PCIe | | 0 | Software control | 3 |
| 11 | | | | | |
| MOD_SRIO | SRIO | | 1 | Software control | 4 |
| 12 | | | | | |
| MOD_HyperLink | HyperLink | | 0 | Software control | 5 |
| 13 | | | | | |
| MOD_L2SRAM | L2SRAM | | 0 | Software control | 6 |
| 14 | | | | | |

# Clock Domains: KeyStone Wireless Applications

| | | | | | |
|---|---|---|---|---|---|
| MOD_MSMCSRAM | 15 | MSMCSRAM | 0 | Software control | 7 |
| MOD_RAC | 16 | RAC_A+RAC_B+MPU4 for RAC | 0 | Software control | 8 |
| MOD_TAC | 17 | TAC | 0 | Software control | 8 |
| MOD_FFTC | 18 | FFTC | 0 | Software control | 9 |
| MOD_AI | 19 | AIF2 | 1 | Software control | 10 |
| MOD_TCP3D | 20 | TCP3d | 0 | Software control | 11 |
| MOD_VCP2_B | 21 | VCPB | 0 | Software control | 12 |
| MOD_VCP2_C | 22 | VCPC | 0 | Software control | 12 |
| MOD_VCP2_D | 23 | VCPD | 0 | Software control | 12 |
| MOD_CorePac0 | 24 | CorePac0+local timer | 0 | Software control | 13 |
| MOD_CorePac1 | 25 | CorePac1+local timer | 0 | Software control | 14 |
| MOD_RSAx2_1 | 26 | RSAs for CorePac1 | 0 | Software control | 14 |
| MOD_CorePac2 | 27 | CorePac2+local timer | 0 | Software control | 15 |
| MOD_RSAx2_2 | 28 | RSAs for CorePac2 | 0 | Software control | 15 |
| MOD_CorePac3 | | CorePac3+local timer | 0 | Software control | 16 |
| No LPSC | | Bootcfg, PSC, Main PLLCTL. | | These modules do not use LPSC. | 0 |

NOTE: For an IP to be reset isolated, reset isolation needs to be enabled by configuration of one MMR (RESETISO in Module Control Register) in the corresponding LPSC. Boot ROM code configures the MMR to enable reset isolation for SmartReflex, SRIO, SGMII, and AIF2.



# Power States

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# Power State Definitions for IPs

- OFF
  - No power to standalone IP.
  - Modules that have a logic power domain, such as SRIO and PCIe.
  - It is expected that a logic power domain fully power gated will result on a leakage reduction in that power domain in the order of 4x to 10x.
- SRAM-OFF
  - Only memories are powered off
  - This mode requires that the IP be in PSC-CLK_RST_DIS
  - For wake-up, software needs to reconfigure IP to use it.
  - Not apply to CorePac SRAM.
- PSC-CLK_RST_DIS: reset low + clock gated
- PSC-CLK_DIS: clock gated + no-reset-applied
- CorePac_STATIC_PD: CorePac can enter Static Power Down mode by configuring its built-in power down controller (PDC).
- Packet-forwarding
  - IPs support the packet-forwarding mode: SRIO, SGMII and AIF.
  - The packet forwarding mode for SRIO, SGMII and AIF are different. For SRIO, it requires clock alive to provide packet forwarding. However, SGMII and AIF will not depend on clock to provide forwarding function.
- Reset Isolation: IP is in reset isolation state.
- Active: leakage + clock power, dynamic power depending on activity. It could be idle (~0.01%) to maximum activity (100% utilization).

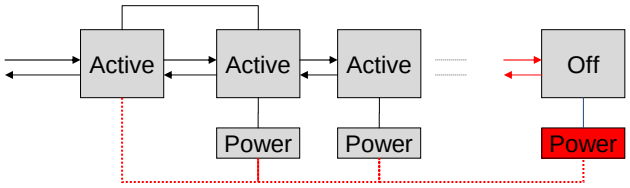


# Power State Definitions for SOC

- OFF - no power to IPs.
  - Power Expectation-no power
- Hibernation2 - requires chip reset to exit, the chip reset is triggered through pin, MSMC + L2 SRAM turned-off.
  - For TCI6616, the response time is less than few seconds. (three modes: AIF, SRIO, SRIO+AIF)
  - For TCI6608, the response time is less than 1~2 seconds. (three modes: SRIO, Ethernet, SRIO+Ethernet)
- Hibernation1 - requires chip reset to exit, the chip reset is triggered through pin.
  - For TCI6616, the response time is less than 100ms. (three modes: AIF, SRIO, SRIO+AIF)
  - For TCI6608, the response time is less than 100ms. (three modes: SRIO, Ethernet, SRIO+Ethernet)
- Standby
  - TCI6616's requirement is to recover from less than 25ms.
  - L2 and MSMC SRAM will be in memory retention mode to meet the timing requirement TCI6608's requirement is to recover from less than 10ms.
  - CorePacs are in static power down, debugss/CP_tracers/TETBs. No LPSC status change when entering/exiting standby.
- Chip Exiting Reset Default - default state after POR or chip level reset.
- Active
  - leakage + clock power, dynamic power depending on activity
  - TCI6616: WCDMA, LTE, LET-A, Geran
  - TCI6608 : HyperLink, SRIO, Ethernet, SRIO+Ethernet, Ethernet + HyperLink+ PCIe, Ethernet + SRIO + PCIe, Ethernet + PCIe, Ethernet + SRIO + PCIe

# Device OFF

- No power supply to device
- Device chains are still connected:
  - GPIO
  - I2C
  - JTAG
  - RIO
  - AIF2
- It is mandatory to maintain the signal chain integrity
- Actual solution: external buffers on critical chains

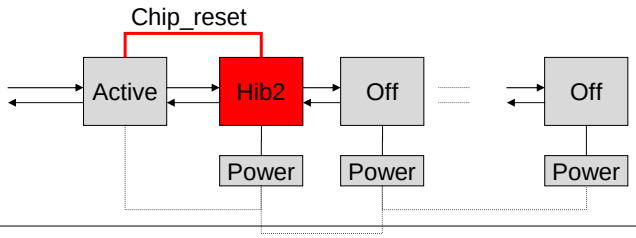





# Hibernation 2: Deep Hibernation

- Exit on chip_reset
- Chip-reset triggered via external pin
- Response time: a few seconds
- Targeted operation modes: Night mode

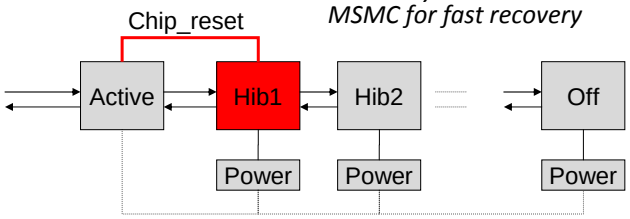
- Characteristics at a glance:
  - MCM, FFTC PDs are OFF
  - L2, MSMC, TCP3d, VCP2 are SRAM-OFF
  - DDR3 in Reset
  - AIF and/or RIO are in Reset Isolation
  - All other IPs in CLK_RST_DIS
  - Cores in STATIC_PD



# Hibernation 1: Light Hibernation

- Exit on chip_reset
- Chip-reset triggered via external pin
- Response time: recovery in less than 100 ms
- Targeted operation modes:
  - Low Traffic mode
  - Active mode

- Characteristics at a glance:
  - MCM, FFTC PDs are OFF
  - L2, TCP3d, VCP2 are SRAM-OFF
  - DDR3 in Reset
  - MSMC is active
  - AIF and/or RIO are in Reset Isolation
  - All other IPs in CLK_RST_DIS
  - Cores in STATIC_PD
- *Possibility to save the states of FL to MSMC for fast recovery*

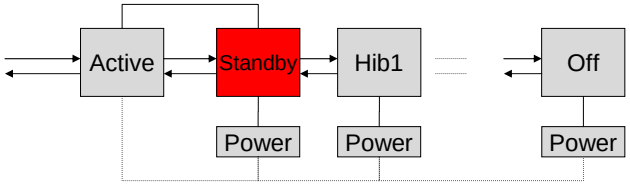




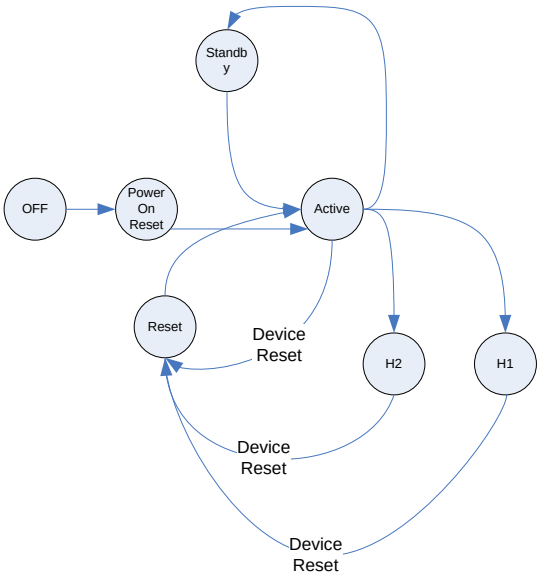

# Standby Mode

- Response time: recovery in less than 25 ms
- Targeted operation modes:
  - Low Traffic mode
  - Active mode

- Characteristics at a glance:
  - MCM, FFTC PDs are OFF
  - TCP3d, VCP2 are SRAM-OFF
  - DDR3 is active
  - L2, MSMC, SGMII, PA_SS are active
  - AIF and/or RIO are in Reset Isolation (or active)
  - All other IPs in CLK_DIS
  - Cores are idle



# Power State Transitions






# Power Mode Example: KeyStone Media Applications

| Power and clock domain | Chip Exiting Reset Default | Hibernation 2: SRIO+Ethernet |
|---|---|---|
| PD-Always-ON | ACTIVE | ACTIVE |
| PD_DEBUG_TRC(RAM_PSM) | SRAM-OFF | SRAM-OFF |
| PD_NETCP | OFF | ON |
| PD_PCIEX | OFF | OFF |
| PD_SRIO | OFF | ON |
| | | |
| PD_HyperLink | OFF | OFF |
| PD_L2SRAM (RAM_PSM) | ON | OFF |
| PD_MSMCSRAM (RAM_PSM) | ON | OFF |
| LPSC_CorePac0 | ACTIVE | CLK_RST_DIS |
| LPSC_CorePac1 | ACTIVE | STATIC_PD |
| LPSC_CorePac2 | ACTIVE | STATIC_PD |
| LPSC_CorePac3 | ACTIVE | STATIC_PD |
| LPSC_CorePac4 | ACTIVE | STATIC_PD |
| LPSC_CorePac5 | ACTIVE | STATIC_PD |
| LPSC_CorePac6 | ACTIVE | STATIC_PD |
| LPSC_CorePac7 | ACTIVE | STATIC_PD |
| LPSC_SHAREDRST | ACTIVE | ACTIVE |
| LPSC_DEBUGSS | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_TETB_TRC | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_CP_TRACER | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_SRc3_PWR | ACTIVE | ACTIVE+RST-ISO |
| LPSC_EMIF4F | ACTIVE | ACTIVE |
| LPSC_EMIFA_SPI | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_TSIP | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_PKTPROC | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_SGMII | CLK_RST_DIS | FORWARDING?+ RST-ISO |
| LPSC_SA | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_PCIEX | CLK_RST_DIS/active | CLK_RST_DIS |
| LPSC_SRIO | CLK_RST_DIS | FORWARDING+ RST-ISO |
| LPSC_HyperLink | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_L2SRAM | ACTIVE | CLK_RST_DIS |
| LPSC_MSMCSRAM | ACTIVE | CLK_RST_DIS |

## Power Mode Example: KeyStone Wireless Applications

| Power and clock domain | Chip Exiting Reset Default | Hibernation 2: AIF |
|---|---|---|
| PD-Always-ON | ON | ON |
| PD_DEBUG_TRC(RAM_PSM) | SRAM-OFF | SRAM-OFF |
| PD_NETCP | OFF | OFF |
| PD_PCIEX | OFF | ON |
| PD_SRIO | OFF | ON |
| | | |
| PD_HyperLink | OFF | OFF |
| PD_L2SRAM (RAM_PSM) | ON | OFF |
| PD_MSMCSRAM (RAM_PSM) | ON | OFF |
| PD_RAC_TAC | OFF | OFF |
| PD_FFTC | OFF | OFF |
| PD_AI (RAM_PSM) | SRAM-OFF | ON (RST-ISO) |
| PD_TCP3D (RAM_PSM) | SRAM-OFF | SRAM-OFF |
| PD_VCP2 (RAM_PSM) | SRAM-OFF | SRAM-OFF |
| | | |
| LPSC_CorePac0 | ACTIVE | CLK_RST_DIS |
| LPSC_CorePac1 | ACTIVE | STATIC_PD |
| LPSC_CorePac2 | ACTIVE | STATIC_PD |
| LPSC_CorePac3 | ACTIVE | STATIC_PD |
| LPSC_SHAREDRST | ACTIVE | ACTIVE |
| LPSC_DEBUGSS | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_TETB_TRC | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_CP_TRACER | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_SRc3_PWR | ACTIVE | ACTIVE+RST-ISO |
| LPSC_RSAx2_0 | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_RSAx2_1 | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_EMIFA | ACTIVE | ACTIVE |
| LPSC_TCP3E | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_VCP2_A | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_PKTPROC | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_SGMII | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_SA | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_PCIEX | CLK_RST_DIS/active | CLK_RST_DIS |
| LPSC_SRIO | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_HyperLink | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_L2SRAM | ACTIVE | CLK_RST_DIS |
| LPSC_MSMCSRAM | ACTIVE | CLK_RST_DIS |
| LPSC_RAC | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_TAC | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_FFTC | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_AI | CLK_RST_DIS | FORWARDING+CLK_DIS+ RST-ISO |
| LPSC_TCP3D | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_VCP2_B | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_VCP2_C | CLK_RST_DIS | CLK_RST_DIS |
| LPSC_VCP2_D | CLK_RST_DIS | CLK_RST_DIS |

# SmartReflex

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# SmartReflex

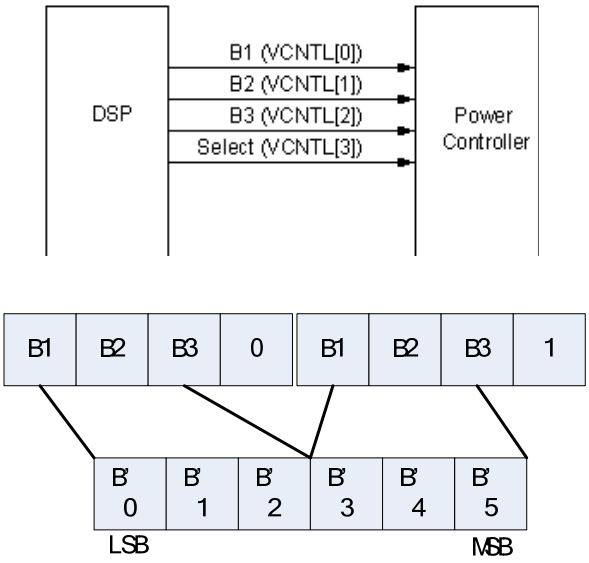
- Some applications require SmartReflex Class 3.
- Class-0 is also supported:
  - NOTE: The VCNTL values have changed from 4 bits to 6 bits. The pin interface has 3 pins plus a select to control high and low bits.
- SmartReflex Class 3 devices:
  - Continuously adjust the supply voltage to changing environmental conditions. Class 0 was fixed based only on process.
  - SmartReflex changes the voltage based on performance requirements. A fundamental requirement is the ability to re-program the power supply.



# SmartReflex VID Control System

- Since SmartReflex™ changes the voltage based on performance requirements, a fundamental requirement is the ability to re-program the power supply. VID (VCNTL) and $I^2C$ (Class 3 only) are standard interfaces. A 4 pin (6 bit) VID (VCNTL) interface and an $I^2C$ interface are required.
- The preferred embodiment of the VID implementation requires 6 bits. The additional 2 bits (6 total) provide for better resolution or granularity during SmartReflex™ operations. A parallel control scheme is implemented to achieve based on 4 pins VID (VCNTL) interface.

# SmartReflex VID Control System






# For More Information

- Refer to the Power Management User Guide
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community website.